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WAVETEK

WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123

INSTRUCTION MANUAL

MODEL 21
11 MHz STABILIZED
FUNCTION GENERATOR

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SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

The instrument power receptacle is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference: ⏚ or ⚠ stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.

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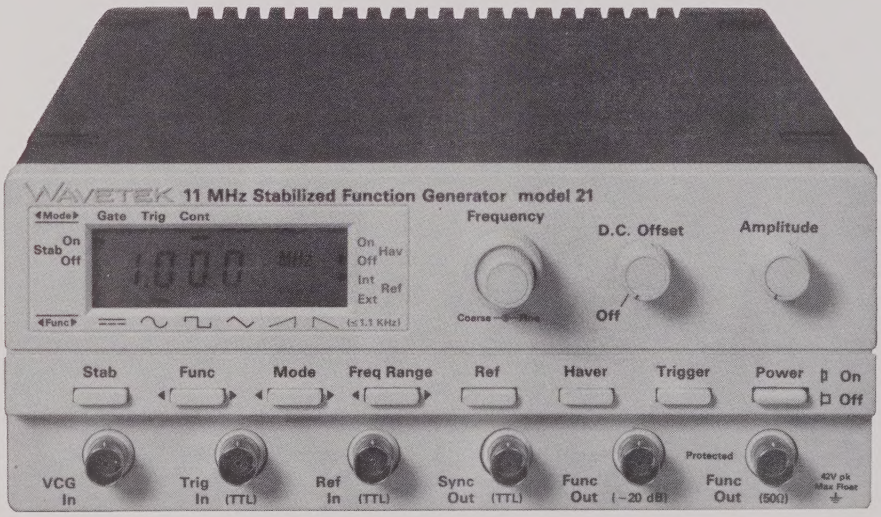

WAVETEK 11 MHz Stabilized Function Generator model 21
Mode
Gate Trig Cont
Stab On Off
On Off Hav
Int Ext Ref
Func
(≤1.1 KHz)
Frequency
Coarse Fine
D.C. Offset
Off
Amplitude
Stab
Func
Mode
Freq Range
Ref
Haver
Trigger
Power On Off
VCG In
Trig In (TTL)
Ref In (TTL)
Sync Out (TTL)
Func Out (−20 dB)
Protected
Func Out (50Ω)
42V pk Max Float

SECTION 1
GENERAL DESCRIPTION

1.1 Model 21

Model 21 is a closed-loop, frequency stabilized, function generator. Both short term and long term frequency accuracies are 0.09% over its 100 μHz to 11 MHz frequency range.

Modes are continuous, triggered and gated. Output levels are to 20V peak-to-peak (10 Vp-p into 50Ω).

Waveforms are sine, triangle, square, ramp up, ramp down, haversine, havertriangle and dc. Above 1.1 kHz waveforms are analog generated; below, waveforms are digitally synthesized. Synthesized waveforms can be held at any point and continued from that point.

Synthesized output signal frequency is 1/1000 of reference clock frequency, which can be internal or external. By use of an external reference clock, the output range can be extended to ultra-low frequencies.

An LCD display shows frequency (3½ digits plus unit of measure) and annunciators that indicate selected operating modes, etc. Output is reverse power protected.

1.2 SPECIFICATIONS

1.2.1 Versatility

Waveforms

A bidirectional switch selects sine (∿), triangle (∿), square (⊓) and dc (⎓). For frequencies below 1.100 kHz ramp up (◿), ramp down (◺) and haverwaves(⩘ , ⩔) are also available.

Operational Modes

Continuous: Generator runs continuously at selected frequency.

Triggered: Generator is quiescent until triggered by external signal or manual trigger, then generates one complete waveform cycle at selected frequency.

Gated: As triggered mode, except output continues for duration of gate signal. Last waveform started is completed.

Frequency Range

100 μHz to 11 MHz in 9 overlapping decade ranges. Range switching with bidirectional switch with frequency digits; decimal and units displayed on LCD display. Each decade range capable of 1100:1 frequency change controlled by the Frequency Coarse and Fine controls.

Function Output

Waveform amplitude variable over a 20 dB range up to 20 Vp-p (10 Vp-p into 50Ω) at Function Out. Waveform also present at Function Out (-20 dB) with a fixed 20 dB attenuation relative to the Function Out for a full 40 dB of amplitude range. Peak output current is 100 mA maximum at Function Out. Source impedance of both outputs is 50Ω.

DC Offset and DC Output

Waveform offset and dc output variable with DC Offset control with off position for calibrated zero offset. Function Out is ± 10V maximum (± 5V into 50Ω) as offset or Vdc output. Signal peak plus offset limited to ± 10V (± 5V into 50Ω). DC offset plus waveform attenuated proportionately at Function Out (-20 dB).

Sync Output

TTL pulse (50% duty cycle) at generator frequency will drive 10 LS TTL loads.

VCG — Voltage Controlled Generator

Up to 1100:1 frequency change with external 0 to ± 5V signal applied to VCG IN connector. Upper and lower frequencies limited to maximum and minimum of selected range. Input impedance is 5kΩ and maximum slew rate is 0.1V/μs. VCG IN is disconnected when the Stabilizer is engaged.

Trigger and Gate

External TTL compatible signal at Trig In BNC triggers or gates generator output when generator is in trigger or gate mode. Generator triggers on positive edge of input or gates on for duration of high level input. External signal pulse width is 50 ns minimum with a maximum repetition rate of 5MHz.

Stabilizer

When selected, the generator frequency is stabilized at the displayed frequency to a crystal-controlled reference. The Stabilizer improves long term frequency stability for all durations to be equal to the 10 min. short term value.

When the stabilizer is on, the generator frequency is corrected to the displayed frequency ± 0.09% of range over the entire operating temperature range of 0 to + 50°C. The stabilizer is automatically turned off when the mode is taken out of continuous or Ext Ref. is enabled.

Display

1100 count LCD frequency display with frequency ranging units (mHz, Hz, kHz, and MHz) and decimal point. Annunciators indicate selection of waveform, stabilizer and external reference status, haverwave selection and generator mode.

External Reference

External Reference switch provides selection of internal or external control of waveform output frequency and also provides a means of holding or releasing the waveform manually, electrically or through external contact closure. External Reference connector accepts either a TTL compatible signal (1.1 MHz maximum repetition rate, 200 ns minimum pulse width) or contact closure. External reference provides four modes of operation.

Int Ref: Normal waveform function generator operation when in internal reference and the Ext Ref BNC is either left unconnected or connected to + 5 Vdc or a TTL high.

Ext Ref: External Reference operation by applying frequency to the Ref In BNC with external reference selected. Frequency input controls frequency of the selected waveform at the output. The output frequency will be 1/1000 the reference frequency. Maximum output frequency is 1.100 kHz. When external reference is selected, the display is disabled and blanked.

Manual Hold: At any point on the output waveform by use of the Ref button. Reference mode must be "Int Ref" as above. When Ref button is pressed, the output is stopped. When pressed again, the waveform will start again exactly where it stopped.

Electrical Hold: At any point on the output waveform:

When in "Int Ref" operation and 1.100 kHz or below, hold the waveform by applying 0 Vdc or a TTL low to the Ext Ref BNC or through remote contact closure shorting out the BNC.

When in "Ext Ref" operation, hold the waveform by removing the external signals at Ext Ref BNC or bringing it to 0 Vdc.

1.2.2 Frequency Precision

Frequency Display Accuracy

± 1 count of 1100 counts, which is 0.09% of range. Stabilizer maintains same reading indefinitely.

Time Symmetry

Square waveform variation from 1100 to 100 counts on display less than:

± 0.1% to 1.100 kHz (across bottom five specified ranges),
± 1% to 110.00 kHz,
± 5% to 11.00 MHz.

1.2.3 Amplitude Precision

Sine Variation with Frequency

Less than:

± 0.2 dB on all ranges up through the 10.0 to 110.0 kHz range,
± 1.5 dB to 11.00 MHz.

Referenced to 1 kHz.

1.2.4 Waveform Characteristics

Sine Distortion

Less than 0.5% THD up through the 1.00 to 11.00 kHz range and less than 1% THD up through the 10 to 110.0 kHz range. All harmonics 40 dB down from the fundamental across the 100 to 1100 kHz range and 28 dB across the 1.00 to 11.00 MHz range.

Triangle Linearity

Greater than 99% to 110 kHz.

Square Wave Rise and Fall Times

Less than 22 ns at Function Out with 10 Vp-p output into 50Ω.

Square Wave Total Aberrations

Each peak less than 5% of p-p amplitude

1.2.5 General

Output Protection

Function outputs are protected against a short circuit to any voltage between ± 10V dc and also have internal fused protection (both output and common conductors) against accidental application of up to 250 Vac or 350V dc.

Stability

Amplitude, Frequency (Non-Stabilized) and DC Offset: After 30 minute warm-up;

±0.10% of range for 10 minutes,
±0.50% of range for 24 hours.

Frequency (Stabilized): ±0.10% of range for ⩾10 minutes, 0 to 50°C.

Environmental

Temperature Range: 25°C ± 10°C for spec operation, operates 0°C to 50°C, −20°C to +75°C for storage.

Warm-up Time: 20 minutes for specified operation.

Altitude: Sea level to 10,000 ft for operation. Sea level to 40,000 ft for storage.

Relative Humidity: 95% at 25°C and at sea level (noncondensing).

Dimensions

21.1 cm (8.3 in.) wide, 8.6 cm (3.4 in.) high, 30.5 cm (12 in.) deep.

Weight

3.4 kg (7 1/2 lb) net, 4.5 kg (10 lb) shipping.

Power

90 to 128, 180 to 256V, 48 to 66 Hz, less than 35 VA.

NOTE

All specifications apply for display between 1100 and 100 frequency counts; amplitude at 10 Vp-p into 50Ω.

SECTION 2
INITIAL PREPARATION

2.1 UNPACKING INSPECTION

After carefully unpacking the instrument, visually inspect all external parts for possible damage. If damage is discovered, file a claim with the carrier who transported the instrument. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earth ground can be identified at the plug on the instrument power cord; of the three terminals, the earth ground terminal is the nonmatching shape, usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 115 Vac line supply and with a 3/8 amp fuse. If the unit is shipped for 115 Vac operation, there will be no markings or tags on the unit. If the unit is shipped for 220 Vac operation, there will be a 220 Vac tag on the rear panel of the unit.

2.2.2 Verifying the Line Voltage

CAUTION

All calibration pots are located inside the bottom cover on the circuit board. Be careful not to bump any pots, as this may require a recalibration of the instrument. Moving R103, located near the front panel, can keep the generator from operating; if adjustment is needed, refer to table 5-1 steps 1 through 10.

To verify the line voltage (or change the fuse), the operator must first remove the top and bottom covers. Remove the top and bottom using the following steps and figure 2-1.

1. Remove two (2) screws holding top and bottom covers to rear panel.
2. Slide both covers (together as a unit) to the rear and remove from the chassis assembly.

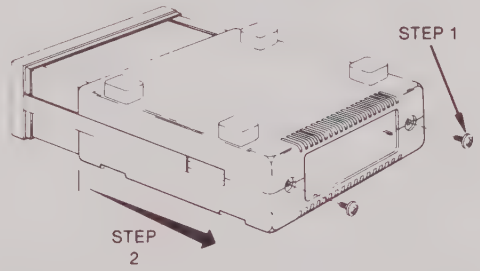


Figure 2-1. Top and Bottom Cover Removal

After the covers have been removed, the line voltage can be checked by viewing the voltage label through the inspection hole as shown in figure 2-2.

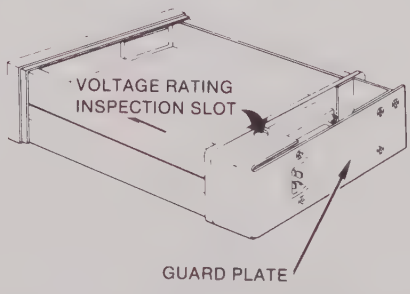


Figure 2-2. Line Voltage Inspection Hole

2.2.3 Fuse and Voltage Selection

If the line voltage is not correct, perform the following steps and refer to figure 2-3 for steps 1 and 2, and figure 2-4 for steps 3 thru 5 to change the line voltage and fuse.

1. Remove the five screws attaching the guard plate.
2. Hold the ac power receptacle assembly against the rear panel while removing the guard plate.

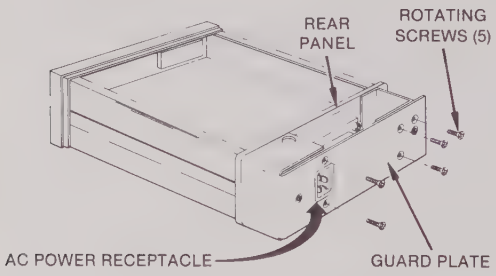


Figure 2-3. Guard Plate Removal

3. Hold the ac power receptacle firmly against the rear panel and remove the voltage selector connector from the ac primary board. Rotate the connector until the correct voltage selector indicator is on top.

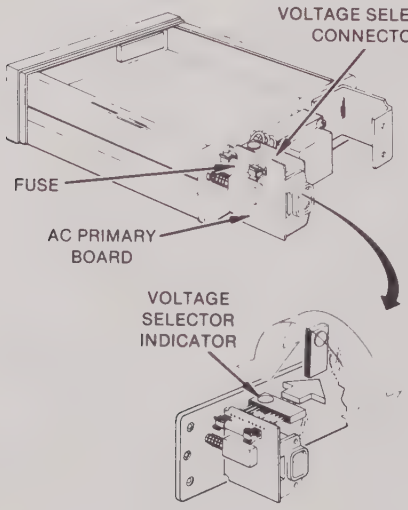


Figure 2-4. Fuse and Voltage Selection

4. Reinstall the voltage selector connector.
5. Remove the fuse and install new fuse as called out in table 2-1.

Table 2-1. Voltage/Fuse Selection

Connector Position	Voltage Range	Fuse
115V	90 to 128 Vac	3/8 amp
220V	180 to 256 Vac	3/16 amp

WARNING

Because lethal voltages are exposed, do not apply ac power to the unit until the guard plate is attached to the unit.

2.2.4 Reassembly

Refer to figure 2-5 for steps 1 thru 5 and figure 2-6 for steps 6 thru 8.

1. Ensure the power rod goes through the slot in the front panel and the ac primary board seats into the slot in the rear panel.
2. Align the guard plate to the ac power receptacle and check the routing of all wires to prevent pinching wires between the transformer and guard plate.
3. Verify that the power rod extends through the front panel slot, the circuit board seats correctly in the rear panel slot.
4. Verify the guard plate, ac power receptacle and rear panel standoffs are properly aligned and then secure with two screws.
5. Fasten the guard plate to the unit with the three remaining screws.

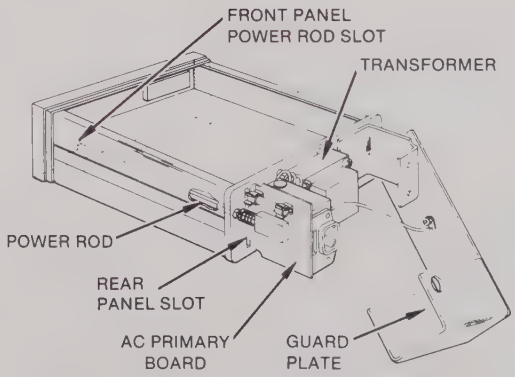


Figure 2-5. Rear Chassis Assembly

CAUTION

When sliding on the bottom cover, avoid pinching any coaxial cables located near the front panel.

6. Turn the instrument upside down, position the bottom cover over the guard shield, and then slide the bottom cover forward approximately two inches while engaging the cover and slides (see figure 2-6, detail A and detail B). Don't slide the cover on yet.
7. Turn the instrument right side up. Install the top cover using the same procedure as in step 6. Don't slide the cover on yet.
8 Align the rear of both the top and bottom cover with each other so that the cover interlocks are properly mated. Once mated, hold the covers firmly together and slide the chassis assembly into the mated top and bottom covers.
9. Secure covers to the chassis assembly using two screws as shown in figure 2-1.

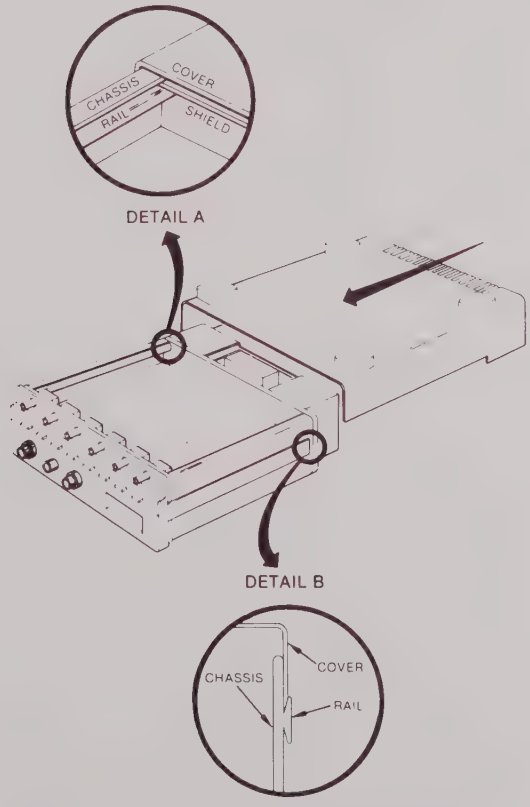


Figure 2-6. Top and Bottom Cover Installation

2.2.5 Signal Connections

Use RG58U 50Ω or equivalent 50Ω coaxial cables equipped with BNC connectors to distribute signals.

NOTE

Signal ground may be floated up to ±42V with respect to chassis ground. Be aware that all signal grounds are common and must all be floated together.

2.3 INITIAL CHECKOUT PROCEDURE

The initial checkout procedure in table 2-2 allows the operator to learn the basic operation and capabilities of the Model 21 in an easy and orderly fashion. In addition, it can be used as a receiving inspection or post-repair checkout. While this procedure verifies functional operation of this instrument, it does not verify the calibration. **The frequencies shown are typical values and should only be used as a guide.** Required tools and test equipment are shown below.

Instrument	Comments
Oscilloscope	Dual channel, 100 MHz bandwidth
Voltage Source	+5Vdc
50Ω Feedthrough	0.5% accuracy, 2W
External Generator	200 Hz to 1.1 MHz TTL output
BNC Tee	1 male, 2 female connector
BNC Coax Cable	RG58U, 3 ft. length (3 each)

2.3.1 Using the Procedure

The checkout procedure (table 2-2) can be used several different ways. It can be started at step 1 and followed straight through to the final step. Or, it can be entered at the highlighted steps, which start specific groups of checks. If the table is being followed in sequence from the previous step, perform the instructions as written. But, if starting from a high lighted step, the Model 21 must be reset to the power on settings (see below). To do this, turn the Power Off, then On.

Power On status:

Frequency Range: 0.001 to 1.100 kHz
Mode: Continuous
Function: Sine
Haver: Off
Reference: Int.
Stabilizer: Off

2.3.2 Front Panel Switches

The Func, Mode, and Freq Range switches are bidirectional. To use these switches, the operator must press the left or right side of the switch's front surface, as

indicated by the arrows on the panel. Pressing the center of any bidirectional switch does not ensure correct operation. All other switches can be pressed anywhere.

When a switch is pressed, either the frequency or an annunciator on the display will change, as shown in table 2-2.

Table 2-2. Initial Checkout Procedure

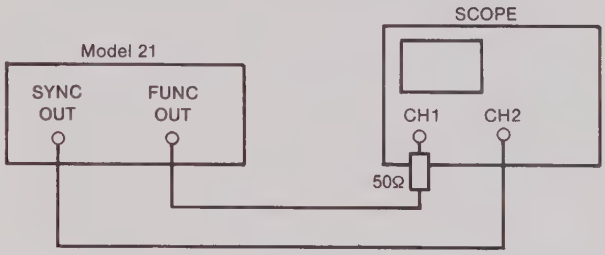
NOTE

1. *Before beginning this procedure, review paragraph 2.3.*
2. *Frequencies shown are typical and should only be used as a guide.*
3. *If starting at a highlighted step, first press Power Off, then On.*

Initial Settings

Control	Setting
Frequency	
Coarse	cw
Fine	cw
Amplitude	cw
D.C. Offset	off

Test Setup 1



Scope	Setting
Time base	0.2 ms/div
CH1 Vert	2V/div
CH2 Vert	2V/div
Trigger	CH2
Display	CH1

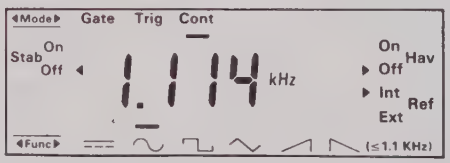
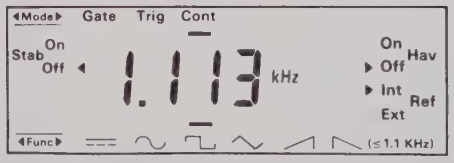
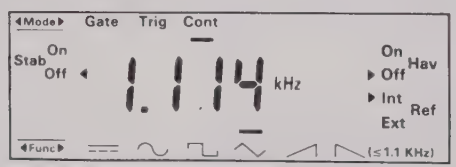
Step	Control	Operation	Display	Observation/Comments
Function Check				
1	Set to Initial Settings Power On			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
2(a)	Func	 Press Once		10Vp-p square wave
2(b)		 Press Once		10Vp-p triangle

Table 2-2. Initial Checkout Procedure (Continued)

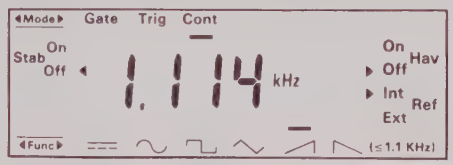
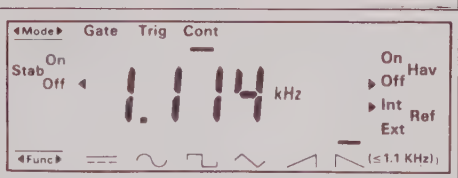
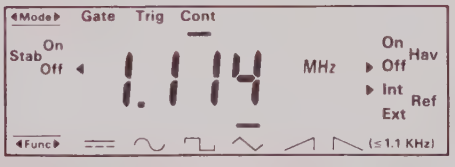
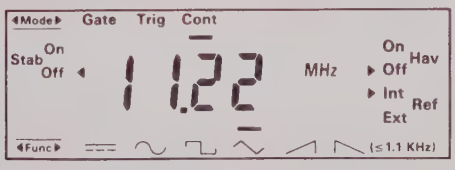
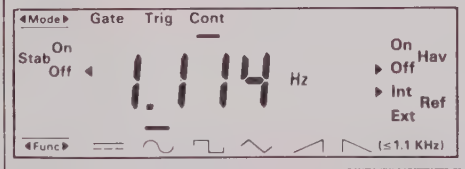
Step	Control	Operation	Display	Observation/Comments
2(c)	Func	Press Once		10Vp-p ramp down.
2(d)		Press Once		10Vp-p ramp down.
Frequency Range Check (11k to 11 MHz)				
3(a)	Freq Range	Press Once		11 kHz, 10Vp-p triangle. Ramp defaults to triangle above the 1.1 kHz range.
3(b)		Press Once		110 kHz.
3(c)		Press Once		1.1 MHz.
3(d)		Press Once		11 MHz.
Frequency Range Check (110 Hz to 110 mHz)				
4	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
	Power	Press to Off then to On.		

Table 2-2. Initial Checkout Procedure (Continued)

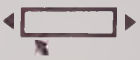
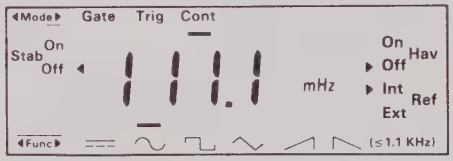
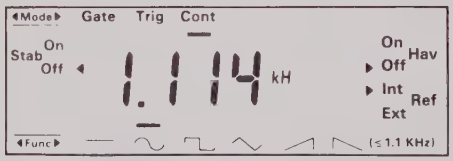
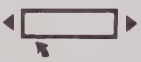
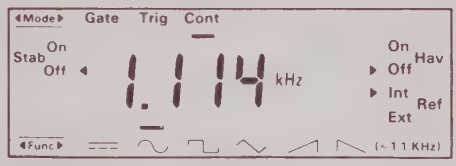
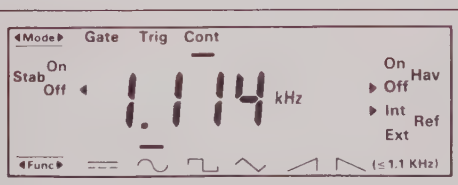
Step	Control	Operation	Display	Observation/Comments
5(a)	Freq Range	Press Once		110 Hz.
5(b)		 Press Once		11 Hz.
5(c)		Press Once		1.1 Hz.
5(d)		Press Once		110 mHz.
DC Offset Check				
	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
	Power	Press to Off, then to On.		
7	Func	 Press Once		0 Vdc.
8(a)	D.C. Offset	Full cw		Greater than +5 Vdc.
8(b)		Full ccw, but not off		Greater than −5 Vdc.

Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
8(c)		Off		0 Vdc
Coarse and Fine Frequency Check				
9	Set to Initial Settings			Connect as shown in test Setup 1. 1.1 kHz, 10 Vp-p sine wave.
	Func	Press Once		
10	Frequency Coarse	Full ccw		Approximately 11:1 frequency change. Verify all display segements function.
11	Frequency Fine	Full ccw		Approximately 100.1 frequency change.
12	Frequency Coarse and Fine	Both full cw		Total frequency change of 1100:1.
Amplitude Check				
13	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave; output level decreases to 1 Vp-p as control is rotated.
	Amplitude	Rotate ccw		

Test Setup 2

Scope	Setting
Time base	0.2 ms/div
CH1 Vert	0.2V/div
CH2 Vert	2V/div
Trigger	CH2
Display	CH1

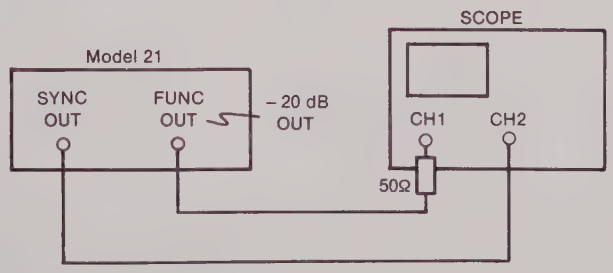
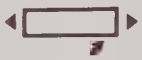
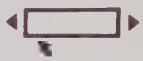
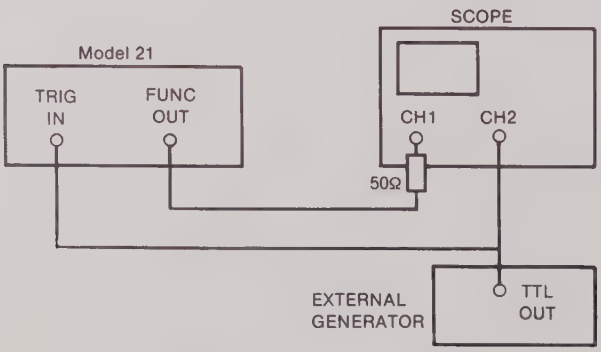


Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
13(b)		Rotate cw		Connect as shown in test setup 2. 1.1 kHz, 1 Vp-p triangle.
Sync Out Check				
14				Display CH2; 1.1 kHz TTL square wave.
Trigger and Gated Check				
15	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10 Vp-p triangle.
	Func	 Press Twice		
16(a)	Mode	 Press Once		Approximately 0 Vdc level.

Test Setup 3



Settings	Scope
Time base	1 ms/div
CH1 Vert	2 V/div
CH2 Vert	2 V/div
Trigger	CH2
Display	CH1 and CH2

External Generator Setting
200 Hz TTL

16(b)		Connect as shown in test setup 3.		CH2: Trigger Input CH1: Triggered Triangle

Table 2-2. Initial Checkout Procedure (Continued)

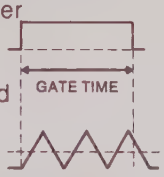
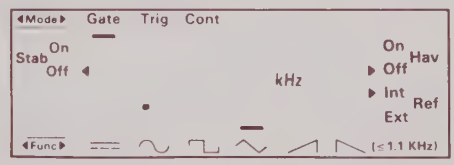
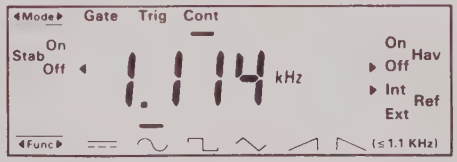
Step	Control	Operation	Display	Observation/Comments
16(c)	Mode	Press Once		CH1: Trigger Input CH2: Gated Triangle
Haver Waveforms Check				
17(a)	Haver	Press Once		CH2: Trigger Input CH1: Gated Haver Triangle 
17(b)		Press Once		Disconnect external generator. Display and Trigger on CH1. Quiescent at negative peak of triangle.
Manual Trigger Check				
18	Trigger	Press and Hold		Continuous triangle while trigger button is pressed.
External Reference Check				
19	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10 Vp-p sine wave.
	Power	Press to Off, then to On.		
20(a)	Ref	Press Once		Quiescent at a dc level

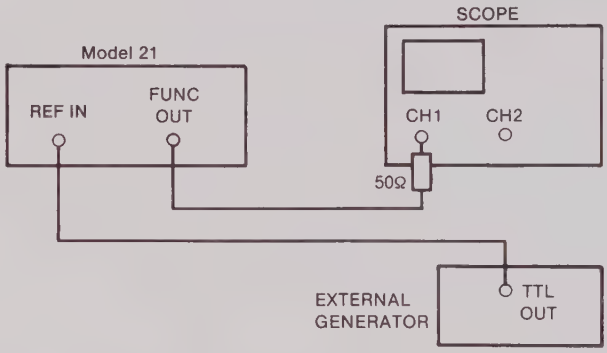
Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments

Test Setup 4

Scope	Setting
Time base	0.1 ms/div
CH1 Vert	2V/div
Trigger	CH1
Display	CH1

External Generator Setting
1 MHz TTL



20(b)		Connect as shown in test setup 4.		1 kHz sine wave. Output frequency tracks the external generator as the frequency is lowered.
20(c)				Disconnect external generator. Quiescent at a dc level.

Stabilizer Check

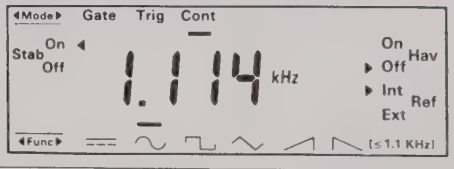
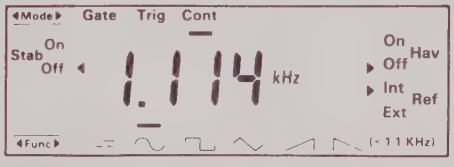
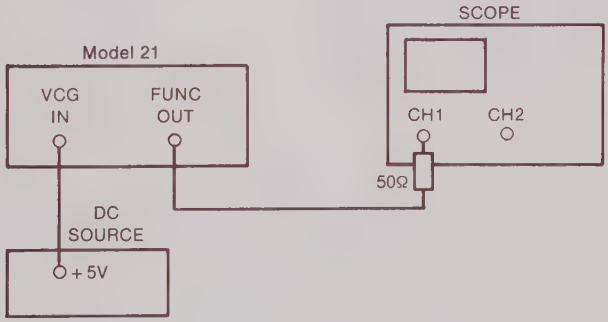
21	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10 Vp-p sine wave.
	Ref	Press Once		
22	Frequency Fine	See Comments		Rotate knob until the least significant digit fluctuates between two digits.
23	Stab	Press Once		The least significant digit remains stabilized.

Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
VCG Check				
24	Set to Initial Settings Stab	 Press Once		1.1 kHz, 10 Vp-p sine wave.
25	Frequency Coarse and Fine	 Both Full ccw		Low frequency sine wave

Test Setup 5

Scope	**Setting**
Time base	0.2 ms/div
CH1 Vert	2V/div
Display	CH1



26	VCG In	+ 5 Vdc		Connect as shown in test setup 5. 1.1 kHz, 10 Vp-p sine wave.

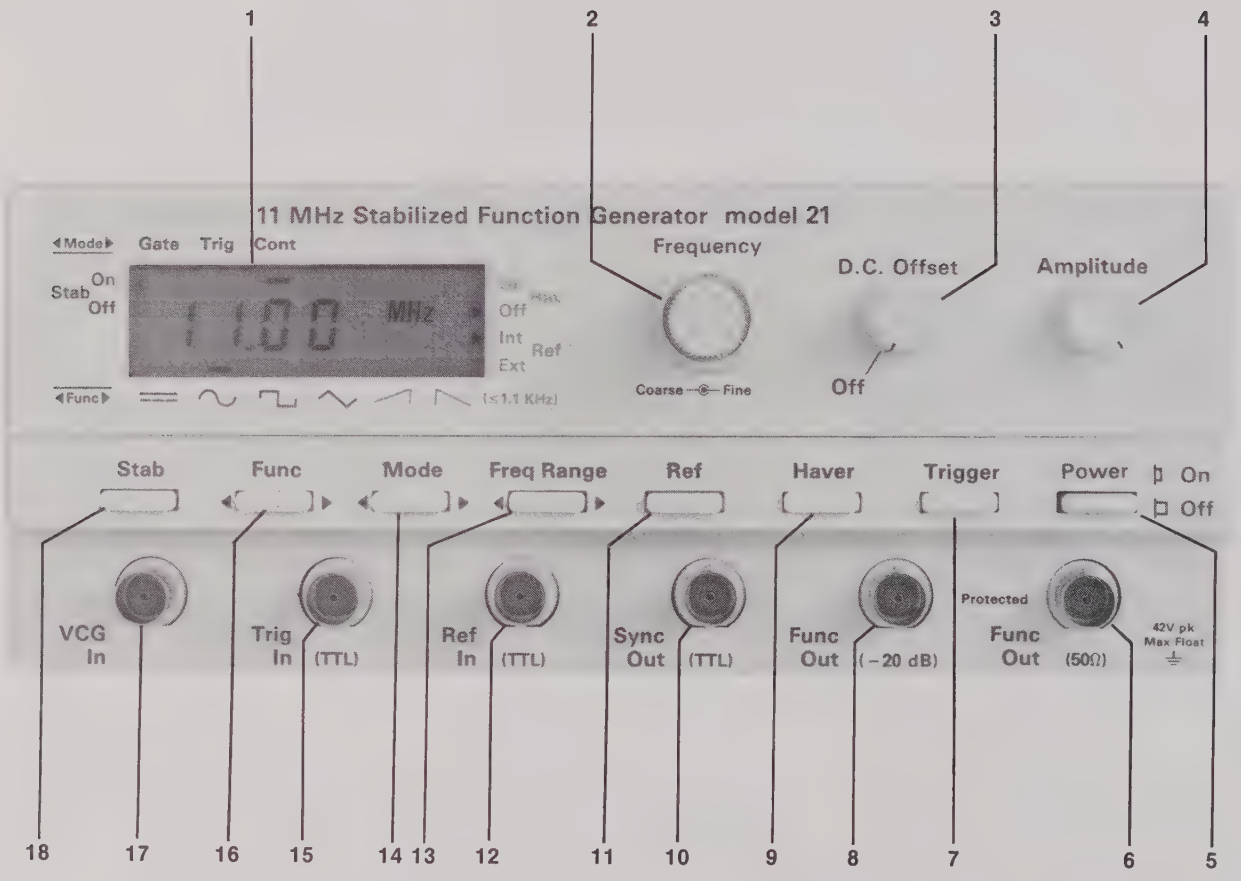


Figure 3-1. Controls and Connectors

SECTION 3
OPERATION

3.1 INTRODUCTION

This section describes the operation of the Model 21. The first part describes the controls and connectors of the instrument. The following parts describe how to use the various functions and modes of the Model 21.

3.2 CONTROLS AND CONNECTORS

The front panel controls and connectors are shown in figure 3-1 and keyed (bold numbers) to the following descriptions.

1 **Display** A 3½ digit (1100 count) LCD frequency display which incorporates annunciators that indicate mode, function (waveform), stabilizer on/off, haverwave on/off, and internal/external reference.

2 **Frequency Controls** Consist of two controls: fine and coarse. The Coarse frequency control, the outer knob of the concentric pair, allows coarse frequency adjustment (approximately 1000 counts) within the selected frequency range.

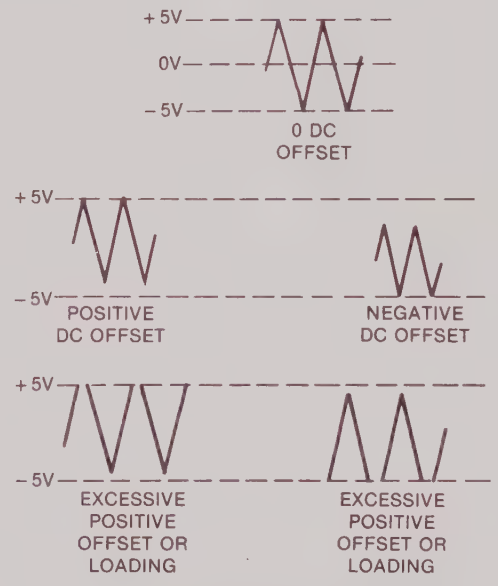
The fine frequency control, the inner knob of the concentric pair, allows fine frequency adjustment (approximately 100 counts) within the selected frequency range. Together the fine and coarse controls provide a range of 1100:1.

3 **D.C. Offset Control** This knob controls the dc voltage and offset of waveforms. A clockwise rotation vertically offsets the waveform up from the normal position (figure 3-2). A counterclockwise rotation vertically offsets the waveform down from the normal position (figure 3-2). A full counterclockwise rotation to Off ensures zero offset.

4 **Amplitude Control** This knob controls waveform amplitudes. Rotate the control full clockwise for maximum amplitude (see table 3-1). A counterclockwise rotation decreases the amplitude by 20 dB.

5 **Power Switch** The power switch turns the instrument On or Off. At power-up the instrument initializes in the following conditions:

Stab: Off
Func: Sine
Mode: Cont
Freq Range: 0.001 to 1.100 kHz
Ref: Int
Hav: Off



Function Out (50Ω) terminated with 50Ω

Figure 3-2. DC OFFSET Control

Table 3-1 Maximum Voltage at Function Out 0 dB

Function	Open Circuit	50Ω Termination
∿ ∿ ⊓	20 Vp-p	10 Vp-p
⊿ ⋀ ⋀		
DC	±10V	±5V

6 **Function Output Connector** This BNC connector is the main output for the selected function. The Amplitude knob **4** controls the amplitude from 1 to 10 Vp-p into a 50Ω load (20 Vp-p into open circuit). Source impedance is 50Ω.

7 **Trigger Button** In triggered mode, the trigger button, when pressed, manually initiates a single cycle of waveform. In the gated mode, it gates the output until the button is released; the last gated cycle will always be completed. The quiescent output depends on the waveform selection and dc offset (see figure 3-3).

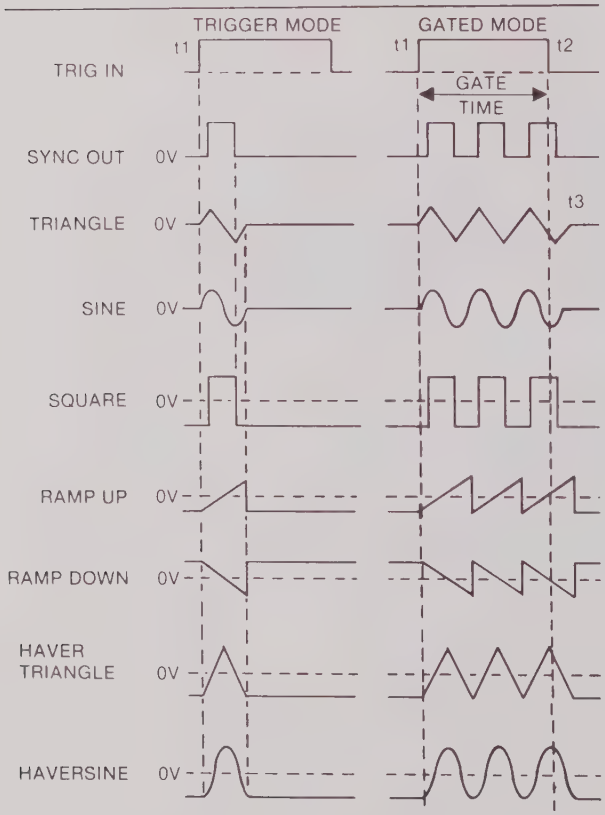


Figure 3-3. Waveforms

8 **Function Output (– 20dB)** This BNC connector is the same as the Func Out **6** except the output is 1/10th (– 20 dB) of the amplitude, 0.1 to 1Vp-p. Both the waveform and offset are attenuated at Func Out (– 20 dB). Source impedance is 50Ω.

9 **Haver Switch** This switch selects either the normal 0° (Haver Off) or – 90° (Haver On) start/stop phase of triggered sine and triangle (figure 3-3). An annunicator on the LCD display **1** indicates the haver status. Haver wave may be selected in the trigger or gates modes using sine, triangle, and square functions on or below the 0.001 to 1.100 kHz frequency range.

10 **Sync Output** This output is a TTL square wave at the frequency of the generator. This output can be used as a synchronizing reference for the Function Outputs **6** and **8**. Phase of the waveforms relative to the sync output is shown in figure 3-3.

11 **Reference Switch** This switch serves two functions: a reference selector or manual hold control.

As a reference selector, the switch selects the reference for the waveform synthesizer, either internal or external. The annunciator on the LCD dipslay **1** indicates the reference status.

As a manual hold control with the internal reference selected and no input or TTL high at Ext Ref BNC **12**, pressing this button stops the waveform. Press the Ref button again to start the waveform.

12 **External Reference Connector** On frequency ranges below 1.100 kHz, the external reference connector serves two functions: first as an external reference input for the waveform synthesizer and second as an electrical hold for the waveform. The input functions when used with the Ref switch **11** are as follows:

External Reference Mode allows the use of an external reference signal for the synthesizer, producing a 1000 step synthesized waveform at 1.100 kHz and below. The input frequency must be 1000 times the desired output frequency; for example, 100 kHz input produces a 100 Hz output. Maximum input frequency is a 1.1 MHz TTL signal.

Manual Hold with the internal reference selected and no input or a TTL high at the Ext Ref BNC, pressing the Ref button **11** stops the waveform. Press the Ref button to again start the waveform.

Electrical Hold can be used for both internal and external reference modes. In internal reference mode, a 0Vdc, TTL low, or contact closure to ground will stop the waveform; + 5V, TTL high, or an open will start the waveform from where it stopped. In external reference, removing the reference signal or supplying 0Vdc stops the waveform; applying the reference signal starts the waveform from where it stopped.

13 **Frequency Range Switch** This switch, when pushed on the left or right, steps through the nine frequency ranges as shown below.

Specified Range	Lowest Obtainable Frequency
11.00 to 1.00 MHz	0.01 MHz
1.100 to 0.100 MHz	0.001 MHz
110.0 to 10.0 kHz	0.1 kHz
11.00 to 1.00 kHz	0.01 kHz
1.100 to 0.100 kHz	0.001 kHz
110.0 to 10.0 Hz	0.1 Hz
11.00 to 1.00 Hz	0.01 Hz
1.100 to 0.100 Hz	0.001 Hz
110.0 to 10.0 mHz	0.1 mHz

The Frequency knobs **2** adjust the frequency within a range. The frequency and range is displayed on the LCD display **1**. Each range has an 1100:1 breadth.

14 **Mode Switch** This switch, when pushed on the left or right, steps through the three operating modes of the instrument.

Continuous Generator runs continuously at the selected frequency.

Triggered Generator is quiescent (quiescent level depends on waveform and offset selected, see figure 3-3) until triggered, when one complete cycle of waveform is generated.

Gated As for triggered except the waveform is continuous for the duration of the gate signal. When the signal stops, the last waveform cycle started is completed.

An annunciator on the display indicates the selected mode.

15 **Trigger In Connector** This connector accepts a positive-going TTL level input (t_1) to trigger and gate the generator, as shown in figure 3-3. A negative-going edge (t_2) ends the gated operation. When triggered, the generator produces one complete cycle for each trigger input. When gated, the generator produces continuous cycles until the gate signal (t_2) is removed; the last cycle started is always completed (t_3).

16 **Function Switch** This switch, when pushed on the left or right, steps through the six functions of the Model 21: sine ∿, triangle ∧, square ⊓, ramp up ⟋, ramp down ⟍, and dc. An annunciator on the LCD display **1** indicates the selected function. Ramps are only available on and below the 1.100 kHz range.

17 **VCG In Connector** This connector accepts 0 to ± 5V ac or dc input signals, which, when summed with a level proportional to the frequency knobs setting, controls the output frequency within the selected range. Positive input levels increase the frequency, while negative inputs decrease the frequency. Frequency excursions of 1100:1 are possible by placing the Frequency knobs to full clockwise (0 to −5V) or counterclockwise (0 to +5V). Input impedance is 5kΩ and it has a slew rate of 0.1V/μs. If frequency stabilization is selected, the VCG In connector is internally disconnected.

18 **Stabilizer Switch** This switch references the generator to an internal standard which maintains the frequency within ± 1 (least significant) digit. An annunciator on the LCD display **1** indicates the status of the stabilizer. The stabilizer works only in the continuous mode and with an internal reference.

3.3 OPERATION

Perform the initial checkout procedure in Section 2 for a feel of the instrument. Any questions concerning individual controls and connectors may be answered in paragraph 3.2. Bold numbers are keyed to figure 3-1. Outputs are shown in figure 3-3.

3.3.1 Signal Termination

Proper signal termination, or loading, of the generator connectors is necessary for its specified operation. For example, figure 3-4 shows proper termination of the Func Out (50Ω) connector. Placing the 50Ω terminator, or 50Ω resistance, in parallel with a higher impedance, matches the receiving instrument input impedance to the coax characteristic and generator output impedance, thereby minimizing signal reflection or power loss on the line due to impedance mismatch.

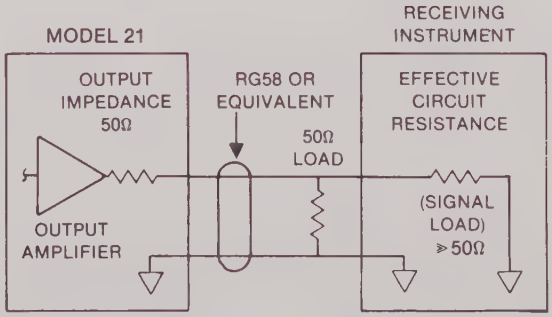


Figure 3-4. Signal Termination

The input and output impedances of the generator connectors are listed below:

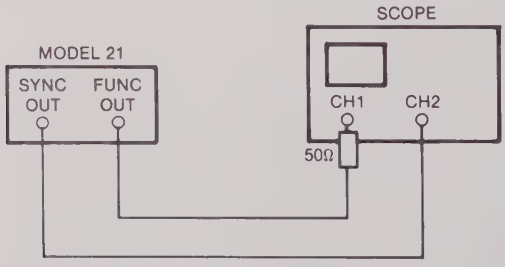
Connectors	Impedance
Func Out (50Ω) **6**	50Ω
Func Out (– 20 dB) **8**	50Ω
Sync Out **10**	TTL
Swp Out **12**	600Ω
Trig In **15**	TTL
VCG In **17**	5kΩ

3.3.2 Continuous Operation

The basic generator supplies a continuous function (waveform) at a fixed frequency set by the operator.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
Mode **14**	Select continuous.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).

To demonstrate continuous operation connect the instruments as shown below, then set the controls as listed below.



Model 21 Settings	Scope Settings
Power: On	Time base: 0.2 ms/div.
Amplitude: cw	CH1 Vert: 2V/div
D.C. Offset: Off	CH2 Vert: 2V/div.
Frequency knobs: cw	Trigger: CH2.
	Display: CH1.

Observation: The scope displays a 1.1 kHz, 10 Vp-p sine wave.

3.3.3 Voltage Controlled Generator (VCG) Operation

VCG is an external electronic means of controlling the frequency of the generator by using signal levels of up to 5V peak. This allows the generator to be swept (up or down in frequency) or frequency modulated.

Control	Setting
Freq Range **13**	Set to the desired frequency range. Frequency can only be changed within a range.
Frequency Coarse and Fine **2**	For positive dc inputs at VCG In, set the Frequency knobs to the lower frequency limit. For negative dc inputs at the VCG In, set the Frequency knobs to a higher frequency limit. For modulation with an ac input at VCG In, set the Frequency knobs at the desired center frequency
VCG In **17**	As required.
Mode **14**	Select continuous.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-3).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).

NOTE

Excessive VCG input voltage may cause nonlinear operation when the generator attempts to exceed the range limits.

The generator can be swept up to 1100:1 with a 5V input signal to the VCG In connector. With the frequency set to 1100, excursions between – 5 and 0V at VCG In provide a 1100:1 decreasing frequency. With the frequency set to 0000, excursions between 0V and + 5V at the VCG

In provide a 1100:1 increase frequency within the frequency range.

The VCG nomograph, figure 3-5 , gives examples of how an input voltage affects the output frequency. Example 1 shows that with 0V VCG input, the Frequency knobs determine the output frequency. Example 2 shows that a positive VCG input increases the output frequencies. Example 3 shows that a negative VCG input decreases the output frequency. In the nomograph decimal points are not shown. The output frequency must be multiplied by the range. For example, in example number 2 if the frequency range is set to the .001 to 1.100 kHz range, the display will read 0.550 kHz and when the VCG voltage is applied the display will read 1.1 kHz.

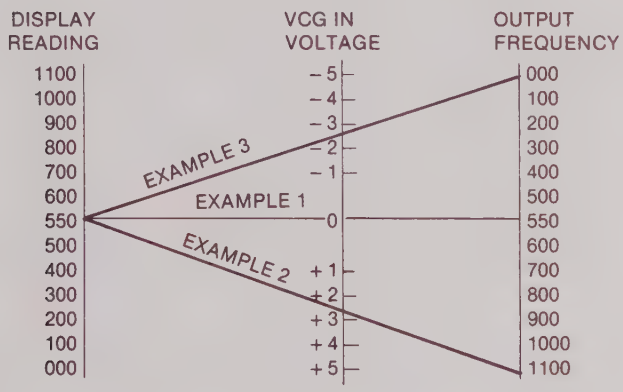
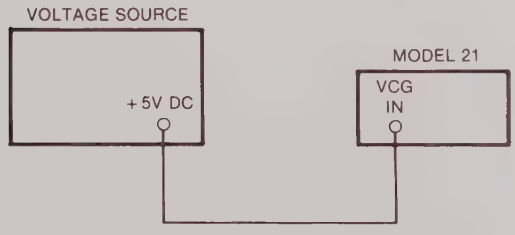


Figure 3-5. VCG Nomograph

To demonstrate VCG operation, connect the instruments as shown below, then set the controls as listed below.



Model 21 Settings	Voltage Source Settings
Power: On	Output level: + 5Vdc.
Frequency knobs: ccw	

Observation: The display reads approximately 1.1 kHz.

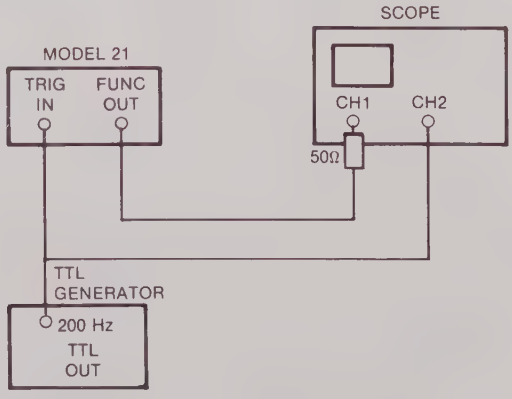
3.3.4 Triggered Operation

A triggered generator produces a single waveform each time a trigger signal is received. The Model 21 can be triggered by manual control or with a TTL signal.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.
Mode **14**	Select Trigger.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Trig In **15**	Connect to TTL signal source at desired trigger repetition frequency (less than Model 21 frequency).
Trigger **7**	Press to trigger.

The triggered waveform starts from a quiescent point (Sine and triangle: 0Vdc; square, ramp up, haver sine, and haver triangle: lower level; ramp down: upper level. All waveforms may be d.c offset). The Model 21 triggers on the rising ( ) edge of the trigger signal.

To demonstrate trigger operation, connect the instruments as shown below, then set the controls as listed below.



Model 21 Settings	Scope Settings	TTL Generator
Power: On	Time base: 1ms/div.	Frequency: 200Hz.
Frequency knobs: cw	CH1 Vert: 2V/div.	Output level: TTL.
Amplitude: cw	CH2 Vert: 2V/div.	
D.C. Offset: Off	Trigger: CH2	
Mode: Trigger	Display: CH1 and 2.	

Observation: Scope Channel 1 displays a single 1.1 kHz, 10Vp-p sine wave coincident with the rising edge of the trigger input signal (CH2).

3.3.5 Gated Operation

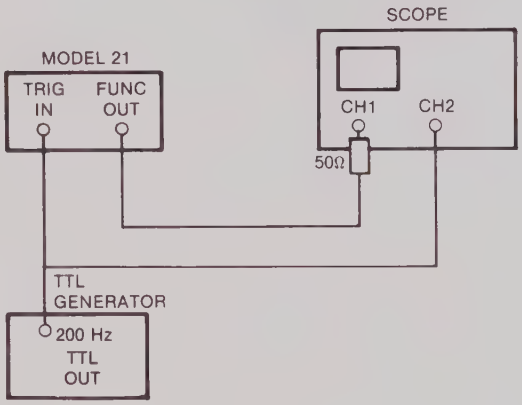
A gated generator produces a continuous output waveform for the duration of the trigger signal. The Model 21 can be gated by manual control (Trig Switch) or with an external TTL signal (Trig In).

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Mode **14**	Select Gate.
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Trig In **15**	Connect to TTL signal source at desired trigger repetition frequency (less than the generator waveform frequency).
Trig **7**	Press in to start gate; release to stop gate.

The gated waveform starts from a quiescent point (Sine and triangle: 0Vdc; square, ramp up, haver sine, and haver triangle: lower level; ramp down: upper level. All waveforms may be dc offset).

The instrument gates from the rising edge (⎍) to the falling edge (⎍) of the Trig In signal. The last cycle started will be completed.

To demonstrate gate operation, connect the instrument as shown below, then set the controls as listed below.



Model 21 Settings	Scope Settings	TTL Generator
Power: On	Time base: 1ms/div.	Frequency: 200 Hz.
Amplitude: cw	CH1 Vert: 2V/div.	Output
D.C. Offset: Off	CH2 Vert: 2V/div.	Level: TTL
Frequency knobs: cw	Trigger: CH2.	
Mode: Gate	Display: CH1 and 2	

Observation: Scope CH1 displays gated sine waves starting at the rising edge of the trigger input (CH2) and ending after the falling edge of the trigger input.

3.3.6 Stabilizer Operation

The stabilizer, when turned on, locks the frequency to the display frequency reading. Stabilizer circuit maintains the generator frequency at this setting. The stabilizer works on all frequency ranges. Thus, the frequency range can be changed without unlocking the stabilizer.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
Mode **14**	Select continuous.

D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Stab **18**	Select On.

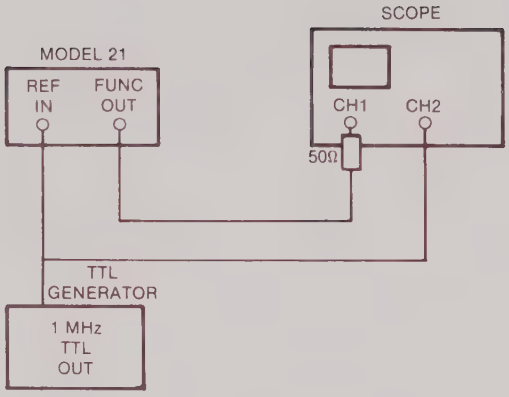
No demonstration of frequency stabilization is given.

3.3.7 External Reference Operation

When external reference is selected with an external reference signal input, the external reference signal controls the instruments frequency. The instrument frequency will be 1/1000 of the reference frequency. Maximum reference frequency is 1.1 MHz TTL signal. This produces a maximum 1.1 kHz output. There is no minimum frequency. Thus, the output frequency can be well below the minimum frequency of the Model 21.

Control	Setting
Mode **14**	Select continuous.
DC Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Ref **11**	Select Ext Ref.
Ref In **12**	Connect to external reference source. 1.1 MHz (maximum) TTL signal.

To demonstrate external reference operation, connect the instruments as shown, then set the controls as listed below.



Model 21 Settings	Scope Settings	TTL Generator
Power: On	Time base: 0.1ms/div.	Frequency: 1MHz.
Frequency knobs: cw	CH1 Vert: 2V/div.	Output level: TTL.
Amplitude: cw	Trigger: CH1	
D.C. Offset: Off	Display: CH1	
Ref: Ext		

Observation: The scope displays a 1kHz, 10Vp-p sine wave. This is 1/1000 the Ref In frequency.

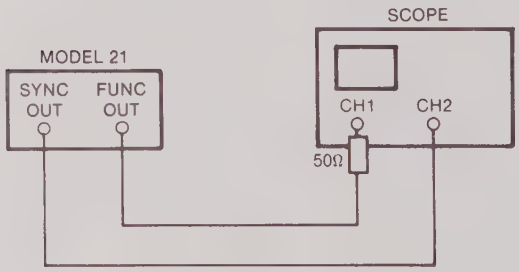
3.3.8 Manual Hold Operation

For manual hold, the Model 21 operates exactly the same as continuous except when the Ref switch **11** is pressed, the waveform immediately stops at a dc level. Pressing the Ref switch again starts the waveform.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range, 1.1 kHz or below.
Mode **14**	Select Continuous.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.

Func Out (50Ω) **6** or Func Out (−20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Ref In **12**	Open circuit, +5Vdc, or TTL high.
Ref **11**	Select external reference to hold and internal reference to restart.

To demonstrate manual hold operation, connect the instruments as shown below, then set the controls.



Model 21 Settings	Scope Settings
Power: On	Time base: 0.2V/div.
Frequency knobs: cw	CH1 Vert: 2V/div.
Amplitude: cw	CH2 Vert: 2V/div.
D.C. Offset: Off	Trigger: CH2.
Ref: As directed	Display: CH1.

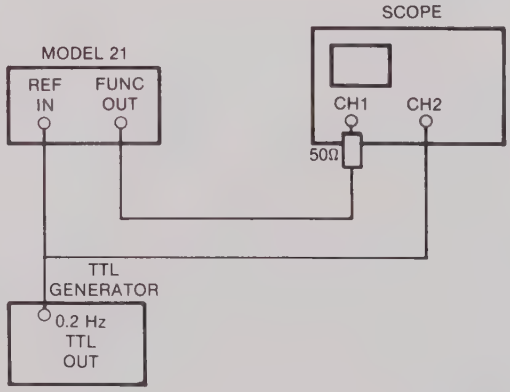
Observation: The scope displays a continuous 1.1 kHz, 10Vp-p sine wave. When the Ref switch **11** is pressed once, the waveform immediately stops at some dc level. press Ref again to resume the waveform.

3.3.9 Electrical Hold Operation

For electrical hold, the Model 21 operates exactly the same as continuous, except the output can be stopped and held at any point.

Control	Setting
Freq Range **13**	Set to the desired frequency range. Must be 1.1 kHz or below.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
Mode **14**	Select continuous.
DC Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (−20 dB).
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (−20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Ref In **12**	For Int Ref operation (1.1 kHz range and below) a contact closure, TTL low, or 0Vdc holds the waveform. An open, TTL high, or +5Vdc releases the waveform. For Ext Ref opeation, (1.1 kHz range and below) removing the reference signal or applying 0Vdc holds the waveform. Connecting the reference signal releases the waveform.
Ref **11**	Set to the desired reference source.

To demonstrate external reference operation, connect the instruments as shown, then set the controls as listed below.



Model 21 Settings	Scope Settings	TTL Generator
Power: On	Time base: 0.1ms/div.	Frequency: 0.2Hz.
Frequency knobs: cw	CH1 Vert: 2V/div.	Output level: TTL.
Amplitude: cw	Trigger: CH1	
D.C. Offset: Off	Display: CH1	

Observation: The Model 21 produces continuous 1.1 kHz, 10Vp-p sine waves when the Ref In signal is high. When the Ref In signal goes low, the output waveform is held at dc level.

SECTION 4
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

The Model 21, an 11 MHz stabilized function generator, operates as an analog waveform generator at frequencies above 1.100 kHz and a digital waveform synthesizer at frequencies below 1.100 kHz. In addition, the frequency, regardless of range, can be stabilized to the display frequency. Refer to figure 4-1.

The function generator loop, controlled by Frequency Coarse and Fine verniers, VCG In, Trig In and the stabilizer, is the heart of the generator. On the four frequency ranges above 11.00 kHz, the function generator loop produces triangle and square waves that are routed directly to the function selector located in the output block; a sine converter, also in the output block, modifies the triangle into a sine wave. The waveform synthesizer produces all the waveforms on the five lower frequency ranges (110.0 mHz, 1.100 Hz, 11.00 Hz, 110.0 Hz, and 1.100 kHz). The waveform can be clocked either internally from the function generator loop through the stabilizer (MFSQ) or externally from an external signal (Ref In). Each clock pulse (MFSQ or Ref In) steps the synthesizer through its 1000 output levels, thus the clock signal is 1000 times the output frequency of the syn-

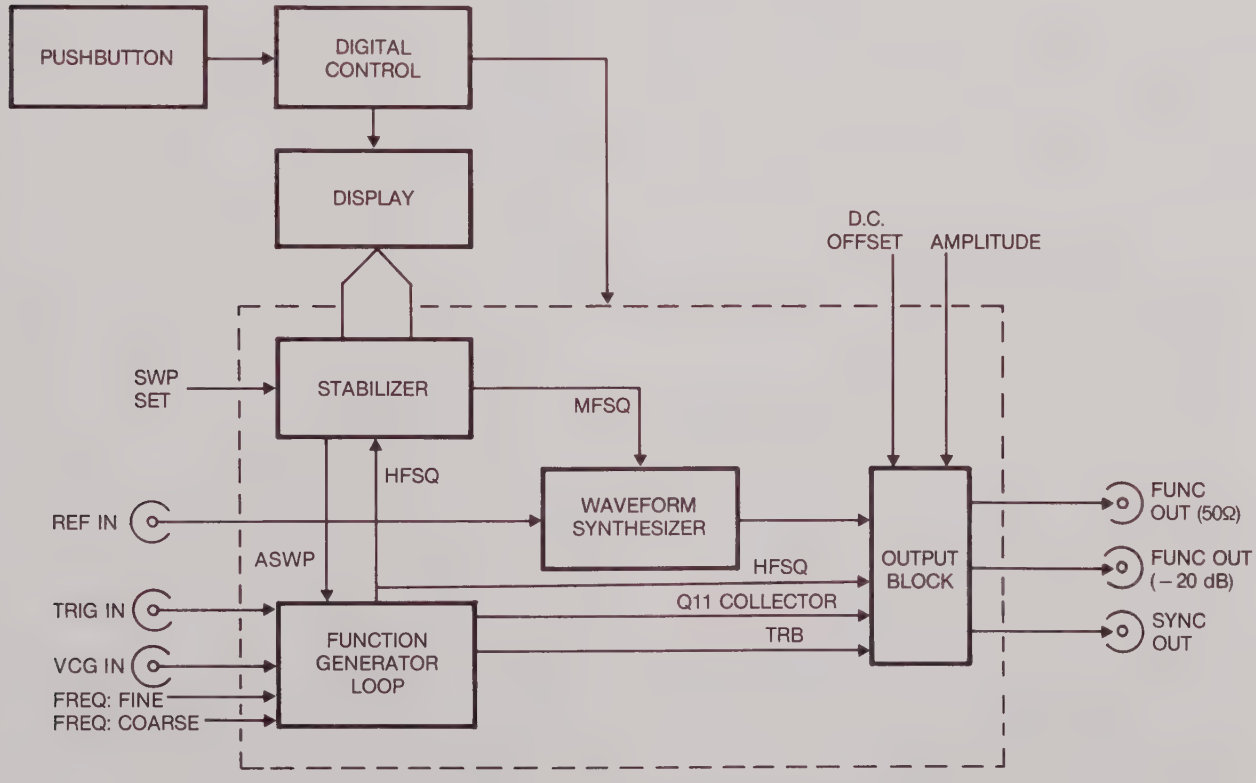


Figure 4-1. Model 21 Block Diagram

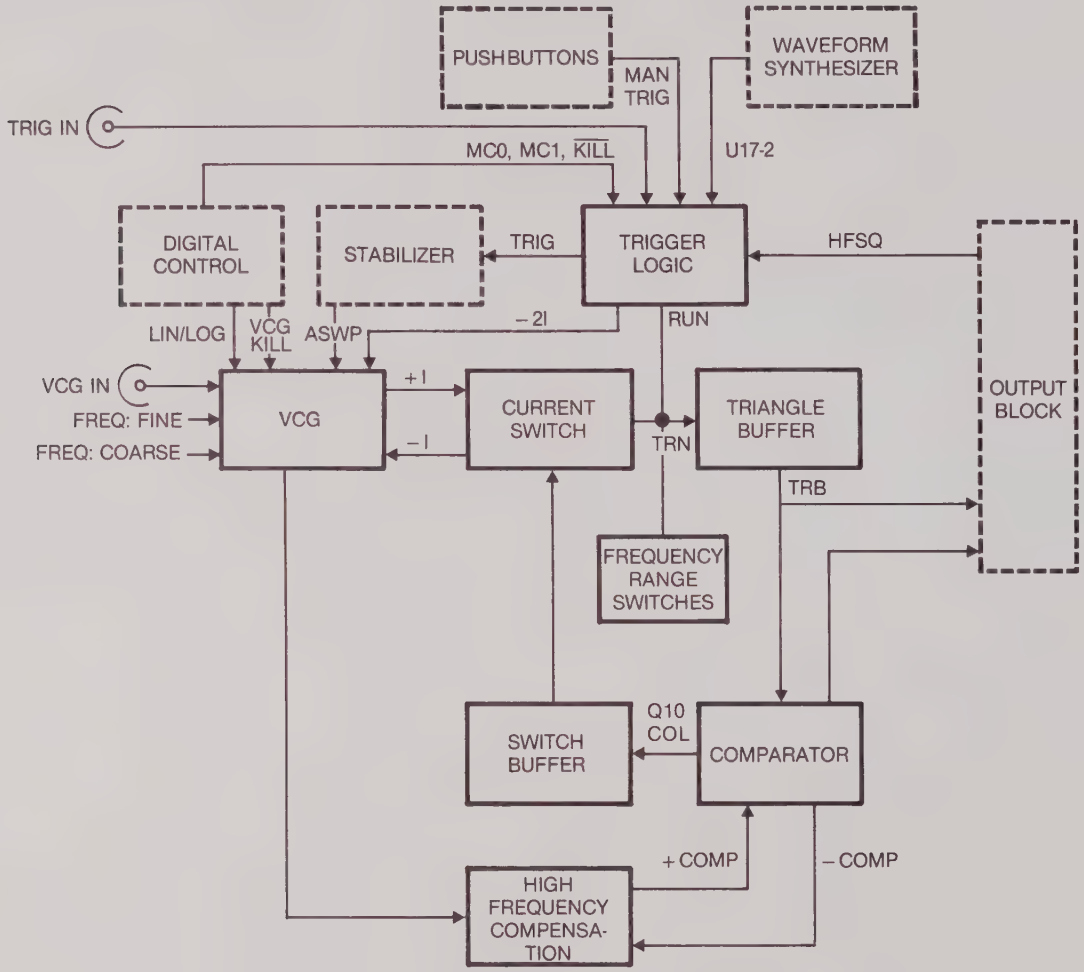


Figure 4-2. Function Generator Loop

thesizer. The synthesizer output, like the higher frequencies, is routed through the function selector. For all ranges, the output block, controlled by the digital control, Amplitude and DC Offset controls, selects and controls the output signal at the Func Out (50Ω), Func Out (−20dB), and Sync Out connectors. When in Stab mode, the stabilizer monitors the frequency output, the same as the frequency shown on the display, from the function generator loop and provides a voltage feedback (ASWP) to the function generator loop, thus keeping the frequency within one least significant count regardless of the frequency range.

The digital control sets the circuits shown in the dotted outline to a default state when the unit is initially turned on. When a pushbutton is pressed, the pushbutton control causes the digital control to change parameters in the appropriate circuit. The digital control along with the stabilizer controls the front panel display.

4.2 DETAILED CIRCUIT DESCRIPTION

4.2.1 Function Generator Loop

Figure 4-2 shows an expanded diagram of the function generator loop that consists of the VCG (voltage controlled generator), current switch, frequency range switches, triangle buffer, comparator, switch buffer, high frequency compensation, and trigger logic circuits.

The VCG produces two currents (+I and −I), alternately switched in and out by the current switch and controlled by the output of the switch buffer which charge (+I) or

discharge (− I) one of four range capacitors in the frequency range switches to produce a linear triangle. The specific frequency is determined by the magnitude of the + I and − I currents. The triangle is amplified by the triangle buffer which drives the comparator that detects the triangle peaks and causes the comparator to switch output states; the threshold level of the comparator is controlled by the high frequency compensation circuit. The output of the comparator controls the switch buffer output state which, in turn, controls the current switch. The function generator loop only produces the top four frequency ranges, the five lower ranges are produced by using the function generator loop to clock the waveform synthesizer. The trigger logic circuit enables or disables the function generator loop depending on the selected mode.

4.2.1.1 VCG

The VCG (ref: schematic 0103-00-1116 sheet 1) consists of the VCG amplifier, current sources, current sink, and trigger control current sink. The VCG amplifier (U1 pin 1) converts voltages from the VCG In (except in Stab mode), FRFINE (frequency fine), FRCOARSE (frequency coarse), into currents that controls the current source and sinks (U28) which set the desired frequency within the selected range. A gain adjustment (R1) controls the top-of-range frequency, while R13 sets the 1100:1 (bottom-of-range) frequency. R11 controls the offset of the amplifier and zener diode CR1 limits the voltage swing at U1 pin 1 to within 30% over the maximum allowable swing. CR2 and CR3 prevent excessive voltages at VCG In from damaging the VCG amplifier.

Current Source and Current Sink: The current source and current sink, part of the VCG circuit, regulate the current leaving the current source, (+ I) and the current entering the current sink, (− I). The negative signal from the VCG amplifier (U1 pin 1) is converted into a current leaving summing node at U1 pin 9 through R1 and R12. U1 pin 8 controls current sunk by Q1 which, in turn, controls current sourced by Q2 and the two transistors in the upper half of U28.

Operational amplifier (U1 pin 8) holds pin 9 at ground potential. When pin 9 tries to go negative, pin 8 goes positive, which causes Q1 to sink current through R18. This lowers the voltage at the base of Q2 and the two transistors in U28 which sources sufficient current through Q2's collector to hold U1 pin 9 at 0V; increased current now flows from the current source (U28 pin 12). CR4 limits the voltage swing at U1 pin 8 to within 30% over the maximum allowable swing.

An increase in current through R42 pin 16 appears like a positive input to the operational amplifier (U1 pin 5) driving the output at pin 7 positive. This raises the voltage at U28 pin 1 that causes pin 3 to sink more current until virtually all the current through R42 pin 16 passes through U28 pin 3, maintaining a virtual ground at U1 pin 5. Increased current now flows into the current sink (− I) through U28 pin 6 which tracks the current source. The emitter resistors for Q4 and U28 pins 2 and 4 are all 1kΩ, therefore the collector currents at U28 pin 3, − I (pin 6), and Q4 will be equal.

Trigger Control Current Sink: The trigger control current sink clamps the triangle node (TRN) at ground potential during the "off" state in the triggered and gated modes.

When the generator is gated "off", RUN goes low, reverse biasing CR7. As the triangle node rises toward the zero crossing point, a greater proportion of the − 2I current emitter resistor at U28 is 500Ω, flows through U3 pin 9. Equilibrium is reached when the trigger holding current is equal to the positive current (+ I) being supplied to the generator loop, preventing the triangle node voltage from rising any further. The matched diodes in U3 have equal currents through them [(− I) + (− I) = (− 2I)] and the anode at pin 4 is grounded, hence the voltage drops across the two diodes are equal and the triangle node is held at ground potential. This stops the triangle waveform on the rising slope and ensures that at least one complete cycle will be generated every time the generator is triggered. Also, refer to paragraph 4.2.1.8 Trigger Logic.

4.2.1.2 Current Switch

The current switch (ref: schematic 0103-00-1116 sheet 2) consists of the diode switches (CR10, 11, 12, 13) current source buffer (Q7) and current sink buffer (Q17). Controlled by the square buffer, it alternately allows the charging (+ I), and discharging (− I) of the selected frequency range capacitor (see paragraph 4.2.1.3) to produce a triangle waveform.

The current switch sources current buffered by Q7 (+ I), or sinks current buffered by Q17 (− I) at the switch output (junction or CR10 and CR12). The instantaneous polarity of the Switch Buffer output control line (junction or R59 and R60) determines the direction of the sinked or sourced current flow.

With the control line at + 2V, CR11 and CR12 are reverse biased and − I current through CR10 linearly charges the selected timing capacitor. At the same time, current flows from the control line through CR13 into the current sink. With the control line at − 2V, CR10 and CR13 are reverse biased. The timing capacitor linearly discharges through CR12 to the current sink and current is sourced through CR11 into the control line.

4.2.1.3 Frequency Range Switches

The frequency range switches (ref: schematic 0103-00-1116 sheet 2) consist of the four basic range capacitors and their controls. Each range capacitor or set of capacitors covers 10% to 100% of full scale. A logic level signal from the frequency range control circuit switches in the range capacitor. For example, when $\overline{FR6}$ goes low, it turns on Q22 which sources about 30 mA through R108 and diodes CR25 and CR26. With CR26 forward biased, the diodes impedance to ground is less than 2Ω and the range capacitor set (C40, C41 and C42) is effectively connected to ground. When this range is not selected, $\overline{FR6}$ is high, Q22 is turned off, and R109 pulls the anode of CR25 to −15V. The voltage divider, R106 and R107, brings the anode of CR26 to −7.5V through the 10 MΩ resistor R105, reverse-biasing CR26. This provides a very high impedance, disconnecting the range capacitor. Frequency range control lines ($\overline{FR4}$ and $\overline{FR5}$) operate the same way by connecting matched capacitors of 0.0047 μF (C43) and 0.047 μF (C45) to the TRN line.

Capacitance for the highest frequency range (100 pF) consists of all the stray capacitance at the triangle node added to C39 and C38 (the 11 MHz adjustment capacitor). Frequency range control line ($\overline{FR6}$) connects an additional 400 pF (C41, C42) and the 1.1 MHz adjustment (C40) to TRN.

4.2.1.4 Triangle Buffer

The triangle buffer (ref: schematic 0103-00-1116 sheet 2), a high speed FET input voltage follower with a low impedance output and unity gain, buffers the current switch and frequency range capacitor from relatively high current circuits in the output block and the comparator.

The triangle buffer consists of Q14, acting as a high input impedance source follower, and Q15, acting as a low output impedance emitter follower. The difference between the input and output voltage of the circuit is controlled by adjusting the current through Q14, such that, the gate-source voltage is equal and opposite to the base-emitter drop of Q15, this causes the two voltages to cancel each other. The baseline adjustment, R103 sets the current through Q14.

4.2.1.5 Comparator

The comparator (ref: schematic 0103-00-1116 sheet 2) detects the peak of the triangle and produces two square wave outputs. One square wave output from the comparator (Q10 collector) drives the switch buffer, while a second square wave of opposite polarity (Q11 collector) drives the output block. The comparator's threshold voltage is set by the +COMP and −COMP from the high frequency compensation circuit.

As the triangle voltage at the base of Q19 reaches the positive threshold voltage (+1V), set by U3 pin 2, Q19 turns on as Q18 turns off. When Q18 and Q19 switch, they also cause the second differential pair, Q10 and Q11, to switch. As Q10 switches "off", current through R63 decreases and the collector of Q10 goes low, (about −1.6V). The current drain through R90 determines the collector voltage of Q10. CR17 and CR18 increase the transistor switching speed of Q18 and Q19 by limiting the signal swing at their collectors to about 0.7V. Resistors R64 and R71 increase the switching speed of Q10 and Q11 by providing a small current which keeps them from turning entirely off, and diodes CR16 and CR19 are switched on and off to further guarantee that Q10 and Q11 do not switch off.

Diode bridge (U3 pins 5, 6, 8) operate similar to the current switch. The switch buffer output (U3 pin 6) state determines the polarity of the comparator threshold at pin 2. The comparator threshold voltage at pin 2 is limited to ±1V by the voltage drop across the 332Ω resistor (R92) since the +COMP and −COMP currents supply no more than 3 mA. The high frequency compensation circuit reduces the +COMP and -COMP currents on the highest frequency range which lowers the comparator threshold voltage at the base of Q18 to compensate for switching delays (see paragraph 4.2.1.7).

Output transistors Q10 and Q11 have different values of collector and emitter resistors to match the input requirements of the buffer that each drives.

4.2.1.6 Switch Buffer

The switch buffer (ref: schematic 0103-00-1116 sheet 2) shifts the level of the comparator's square wave to provide a voltage excursion (±2.2V) capable of driving the current switch. The switch buffer is a complementary emitter follower biased on by the voltage drops across CR14 and CR15 and controlled by the comparator output at the collector of Q10. The ±2.2V square wave output controls the current switch in the generator loop and the polarity of the comparator threshold voltage.

4.2.1.7 High Frequency Compensation

High frequency compensation (ref: schematic 0103-00-1116 sheet 2) circuit sets the threshold voltage of the comparator. On the lower frequency ranges (110.0 mHz through 1.100 MHz), the value of the +COMP and −COMP currents set up the comparator threshold voltage at the base of Q18; each current has a fixed value of 3mA through the resistor R92. On the 1.00 to 11.00 MHz range, the threshold voltage is lowered to compensate for switching delays in the function

generator loop; this maintains the triangle peaks at the same levels as on lower ranges.

On the lower frequency ranges with HF COMP disconnected, R80 and R81 holds U27 pins 2 and 3 and the emitter of Q5 at 0.0V. This puts 15V across series resistors R83 and R85 and −10V at the base of Q16. The same current that flows through R85 also flows through R52. This puts +10V at the base of Q6. The emitter of Q6 is +10.7V which causes 3mA to flow from the collector of Q6 through U3 and R92 to ground during half of the cycle setting up a threshold voltage at the base of Q18. On the opposite half of the cycle, the base of Q18 switches to −1V because the same amount of current (3mA) flows from ground through R92 and U3 to the collector of Q16.

In the 11.00 MHz frequency range, HF COMP (U2 pin 10 of the VCG) is connected to U27 pin 3. At top of the range, 2.5mA is sinked from ground through R80 and R81 to the collector of Q4 in the VCG lowering the voltage at U27 pin 3 to about −5V. This decreases the voltage at the emitter of Q5, as well as the current through R83, R85, and R52 which forces the bases of Q6 and Q16 closer to their respective power supply voltages. The current through R92, the collectors of Q6 and Q16, and the threshold voltage at the base of Q18 are all decreased. This new lower threshold voltage causes the triangle to switch earlier than normal. If the generator is not at full scale, a voltage indirectly proportional to the frequency is set at the base of Q18.

4.2.1.8 Trigger Logic

The trigger logic circuit (ref: schematic 0103-00-1116 sheet 3) allows the generator loop to be externally triggered or gated. When in trigger or gated modes (determined by MC0 and MC1), the trigger logic circuit prevents the generator from running by sinking away the current from the triangle node (TRN) that would normally charge the timing capacitor. Pressing the Trigger button or connecting a signal to the Trig In (TTL) BNC releases TRN which allows the generator to run until HFSQ completes one complete cycle. In addition, the synthesizer output at U22 pin 6 must be high to stop the generator when the frequency range is 1.1 kHz or lower. $\overline{\text{KILL}}$ inhibits the generator when in DC function.

The following paragraphs describe the relationship in various conditions relative to the trigger logic.

Continuous Mode: In Continuous Mode, U12 pin 4 (MC0) is low which holds U12 pin 6 low and sets U23 pin 5 high. $\overline{\text{KILL}}$ (U22 pin 13) will be high for all functions except DC and U22 pin 11 will be low. This sets U23 pin 9 high causing the generator to free-run.

Trig Mode: In Trig Mode, U12 pin 4 (MC0) is held high and U15 pin 4 (MC1) is held low which forces U15 pin 6 and U12 pin 6 high. If the Trigger pushbutton on the front panel is not pressed, U15 pin 10 remains high and U15 pin 10 remains high and U15 pin 8 is in phase with the Trig In signal at U21 pin 13.

With no signal present at Trig In, U23 pin 3 is low. HFSQ is low, U22 pin 8 is high, and U23 pin 5 is low. If $\overline{\text{KILL}}$ (U22 pin 13) is high, U22 pin 11 will be high. U20 pin 10 (LF) is low for frequency ranges 11.00kHz and above which forces U20 pin 8 high. Also, since U22 pin 2 is high, U23 pin 12 is low. Pin 9 will be low disabling the generator.

U15 pin 8 will go high when the Trigger switch on the front panel is pressed (U15 pin 10 goes low) or when an external trigger signal is received (U21 pin 13 goes high). Because the D input at pin 2 is connected to +5V the Q output (U23 pin 5) is high. With $\overline{\text{KILL}}$ (U22 pin 13) high, U22 pin 11 will go low which sets U23 pin 9 (RUN) high and causes the generator to run. At the positive transition of HFSQ (U22 pin 9), U23 pin 11 goes low. On the next negative transition of HFSQ, U23 pin 11 goes high, which clocks the low at pin 12 to pin 9 (RUN) and stops the triangle on its rising edge. Only one cycle of generator output is enabled for each trigger pulse applied.

Gate Mode: In Gate Mode, MC1 (U15 pin 4), MC0 (U12 pin 4), U15 pin 6, U12 pin 6, and U15 pin 10 are high while U23 pin 3 is low. If $\overline{\text{KILL}}$ (U22 pin 13) is high, U22 pin 11 will be high. When LF (U20 pin 10) is low, frequency ranges 11.00 kHz and above, U20 is forced high; because in gate mode $\overline{\text{SWP RUN}}$ is high, U22 pin 3 will be low which disables the generator.

When Trigger on the front panel is pressed (U15 pin 10 goes low) or a voltage at Trig In causes U21 pin 13 to go high, U15 pin 8 also goes high clocking the Q output (U23 pin 5) high. With $\overline{\text{KILL}}$ (U22 pin 13) high, U22 pin 11 will go low which sets U23 pin 9 (RUN) high and causes the generator to run. For the duration of the time the trigger signal at Trig In remains high or the Trigger button is pressed, U15 pin 6 and U12 pin 6 will remain low. This sets U23 pin 5 high, forces U23 pin 10 (S) low, sets RUN (U23 pin 9) high, and enables the generator to free-run.

When U23 pin 3 goes low, U15 pin 6 and U12 pin 6 go high. On the next negative transition of HFSQ, U22 pin 8 goes high which clocks the low at pin 12 to the output at pin 9 (RUN) and stops the triangle oscillation when it reaches 0V.

Low Frequency: When the Frequency range is 1.1 kHz or lower, the trigger logic works much the same as previously described, except U23 pin 12 must be low to stop the generator. This occurs at either the zero crossing of the rising edge of the triangle (Haver Off), or at the negative peak of the triangle (Haver On). If Haver is Off, U13 pin 6 (waveform synthesizer) functions as a zero crossing detector that controls the trigger logic. If Haver is on, U16 (waveform synthesizer) acts as a negative

peak detector. U22 pin 6 goes low in either condition. With U22 pin 6 high, the next positive transition at U17 pin 3 forces $\overline{Q}$ (U17 pin 6) low. For the five lowest frequency ranges, LF (U20 pin 10) is high, this makes pin 8 high and causes U22 pin 3 to go low.

Haver Off: When Haver is Off, HAV (U19 pin 11) is low, which disables U16 and maintains U22 pin 4 high. The zero crossing detector (U13 pin 9) controls the trigger logic; see Low Frequency above.

Haver On: When Haver is on, U19 pin 11 (HAV) is high which disables the zero crossing detector (U13 pin 9). Thus, with HAV high, U16 pin 6 detects the negative peak and controls the trigger logic.

DC Function: If Func is set to DC, U22 pin 13 ($\overline{KILL}$) will be low. This clears U23 and pin 9 (RUN) is forced low, which disables the generator.

4.2.2 Waveform Synthesizer

The waveform synthesizer produces the digitally synthesized waveforms used on the five lower frequency ranges (1.100 kHz and below). It consists of seven circuits: ÷1/÷100 counter, reference selector, ÷1000 up/down counter, waveform EPROM, data selector, latch, and DAC, as shown in figure 4-3 and schematic 0103-00-1116 sheet 3.

The reference selector specifies which reference, external or internal, clocks the 9-bit up/down counter.

External refererence enters through the Ref In BNC. Its frequency must be 1000 times the desired output frequency. Diodes CR40 and CR41 and two inverters (U21) act to prevent damage to the remaining circuitry caused by excessive voltage swings at the Ref In BNC.

The internal reference originates from the function generator loop at HFSQ. This signal must pass through the ÷1/÷100 divider (U7B, U8B; ref: schematic 0103-00-1115 sheet 3) where the frequency is either divided by 1 or 100, depending upon the selected frequency range, see table 4-1.

Table 4-1. Internal Reference Selection

Frequency Range	Generator Loop Frequency (HFSQ)	÷1/÷100	Medium Frequency Square Wave (MFSQ)
.100 to 1.100 kHz	.100 to 1.100 MHz	÷1	1.100 to 1.100 MHz
10.0 to 110.0 kHz	10.0 to 110.0 kHz	–1	10.0 to 110.0 kHz
1.00 to 11.00 kHz	1.00 to 11.00 kHz	–1	1.00 to 11.00 kHz
.100 to 1.100 Hz	10.0 to 110.0 kHz	–100	.100 to 1.100 kHz
10.0 to 110.0 mHz	10.0 to 11.00 kHz	–100	10.0 to 110.0 Hz

This new signal (MFSQ) is 1000 times the output frequency. The control line $\overline{EFC}$ (U15 pin 11) controls the reference selector (ref: schematic 0103-00-1116 sheet 3).

For external reference, $\overline{EFC}$ is held low, which inhibits MFSQ and enables U15 pin 12. The refernce clock, U15 pin 11, is inverted relative to the Ref In signal.

When $\overline{EFC}$ goes high and the Ref In is held high or floats, the internal reference clocks the counter. If Ref In is forced low (external or internal reference), the reference clock (U15 pin 11) is immediately forced high, which stops the clock and holds the synthesizer waveform at a dc level.

The 9-bit up/down counter (U6, U10, U11, and U14) counts from 0 to 499, then reverses and counts from 499 to 0. The counter steering circuit (U11, U16, and U18) watches for the top and bottom counts, then reverses the direction of the counter. When the counter increments, U17 pin 12 is low and pin 8 is high. At the top count, U18 pin 1 toggles high, disabling the counter for one cycle. Also at the top count, U17 pin 12 goes high and on the next clock pulse from U15 pin 11, U17 pin 8 (the counter up/down control line) goes low, causing the counter to begin to decrement, returning U18 pin 1 to its original low state. At the bottom count, U18 pin 1 again goes high, disabling the counter for one cycle. U17 pin 12 goes low, and on the next clock pulse from U15 pin 11, U17 pin 8 goes high, causing the counter to begin to increment. U18 pin 1 again returns low.

The counter output drives the inputs of EPROM (U9) which contains the data needed to produce the sine, triangle, ramp up, and ramp down waveforms. The status of lines FS0 and FS1 determine the waveform by selecting which block of data as accessed; see table 4-2. For sine and triangle waves, the EPROM produces one half cycle, negative to positive peak, on the up count (0 to 499), then uses the same data in reverse, positive to negative peak, on the down count (499 to 0). The data from the EPROM (U9) is latched through U8 to DAC U7.

Table 4-2. EPROM Control Lines

FS0	FS1	Function
0	0	DC
0	0	Sine wave
0	1	Triangle
1	0	Ramp up
1	1	Ramp down

The DAC converts the data from the EPROM into a current, SYNTH SIG, for the function selector.

The synthesizer can also produce ramp up and ramp down waveforms. These ramps are stored in the EPROM (U9), as are the sine and triangle waveforms. To produce the ramps, the line FS0 goes high. The line FS1 selects either the ramp up (FS1 low) or ramp down (FS1 high). In generating the ramps, the up/down counter functions the same as it does for triangles and sine waves; counting 0 to 499 and 499 to 0, except that the least significant bit to the EPROM is controlled by the data selector (U11, U12). The U/D line (U17 pin 9) is the complement of the line that causes the counter to count up or down. When counting up, U/D is low, which holds the least significant bit low. This allows only even addresses to be accessed. When counting down, U/D is high, the least significant bit is held high, and only odd addresses are accessed.

4.2.3 Stabilizer

The stabilizer serves two functions. First, it measures the generator's frequency and drives the frequency display. Second, it compares the displayed frequency,

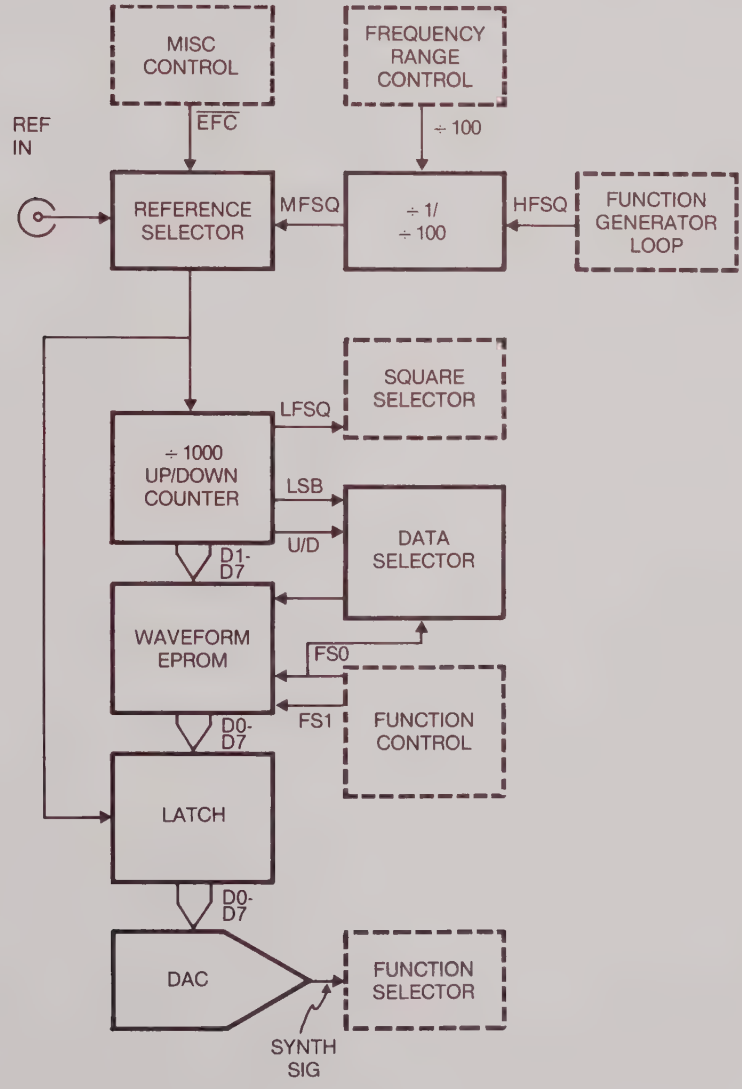


Figure 4-3. Waveform Synthesizer

stored in latches, against the actual frequency of the generator and makes slight frequency corrections to the generator's frequency. Figure 4-4 shows a block diagram of the stabilizer block.

4.2.3.1 Timing Generation

This circuit provides the timing control for the stabilizer. As shown in schematic 0103-00-1115 sheet 2, the 6.4 MHz oscillator consists of crystal (Y1) and differential amplifier (U9A). The output of this oscillator is divided to 50 kHz by U8A (at pin 9).

Four divide-by-10 counters (U5A, U6A) together with their control devices, produce the GATE, MEMCLK, FRCHG, and CLRCNT pulses which control the frequency comparator circuit. Figure 4-5 shows the timing diagram for the counters.

4.2.3.2 Prescalar

The prescalar (ref: schematic 0103-00-1115 sheet 3) selects the clock for the 3½ digit BCD counter. The clock frequency, regardless of the range, will always be 1.00 to 11.00 kHz. The prescalar block consists of the HFSQ divider and selector.

The HFSQ divider (U9C, U8C) divides the HFSQ square wave from the generator loop by 10, 100, and 1000. Each of these outputs drive the selector circuit. In addition,

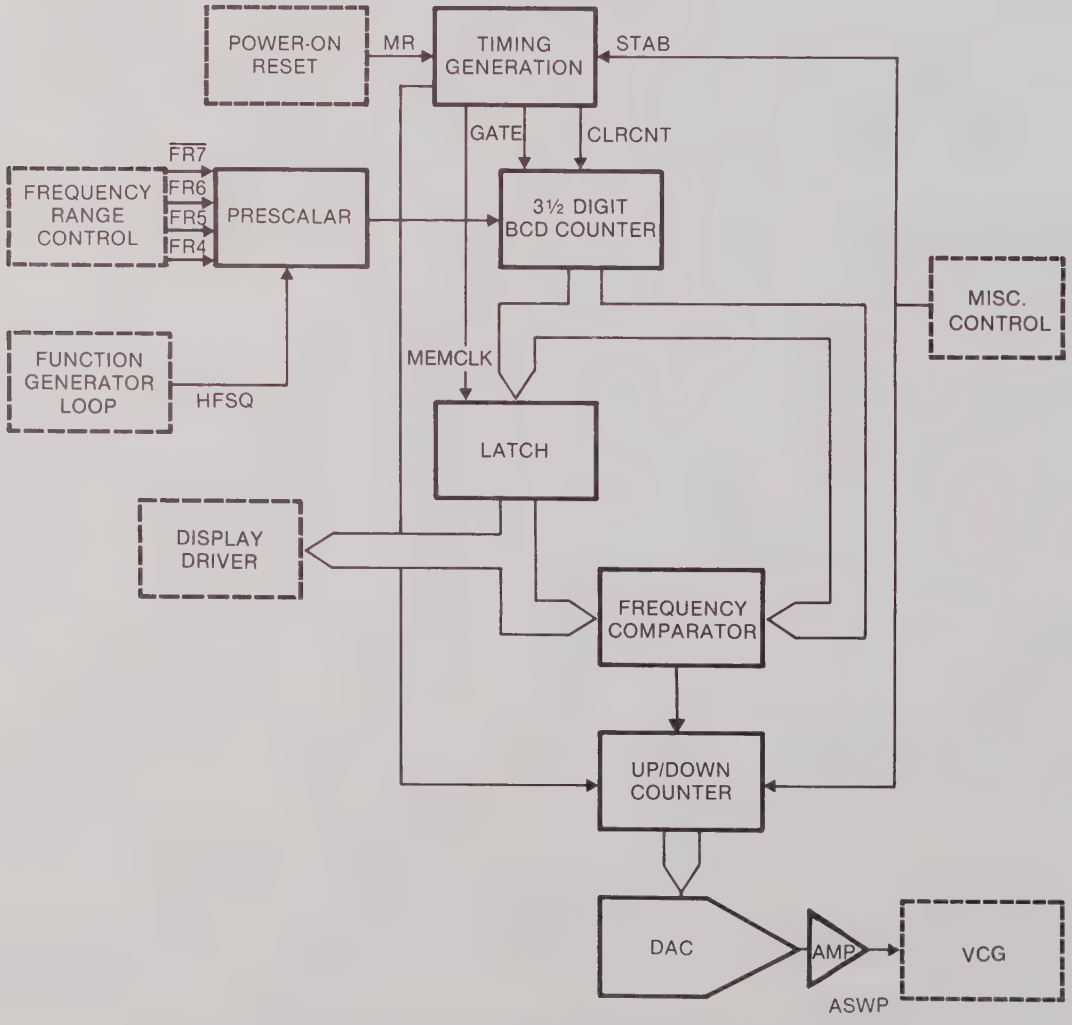


Figure 4-4. Stabilizer Block Diagram

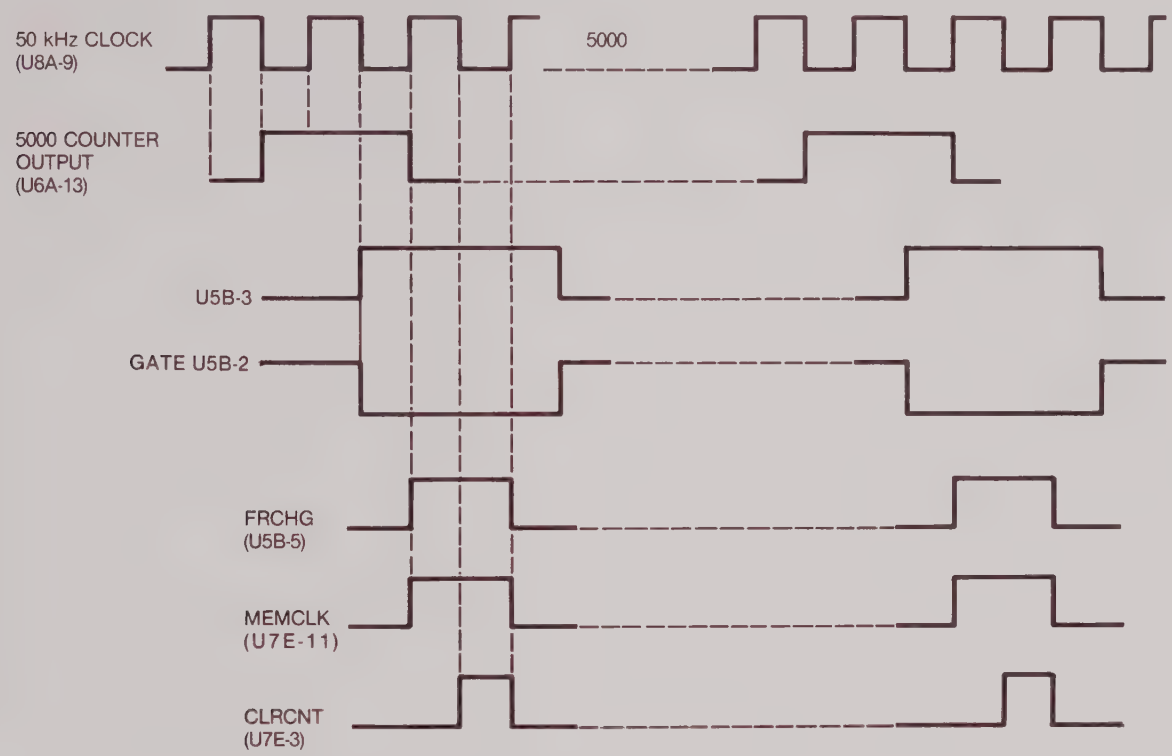


Figure 4-5. Timing Generation

the divider includes the ÷ 1/÷ 100 counter (U7B) for the synthesizer block.

The selector (U9B), controlled by the frequency range control, determines which HFSQ divider output will drive the BCD counter. Table 4-3 shows the relationship between the ranges, generator loop frequency and division ratio.

Table 4-3. Prescalar

Selected Freq Range (Hz)	Actual Function Generator Loop (Hz) Frequency	Divider	Counter Clock (Hz)
1.00 – 11.00 M	1 – 11 M (FR7)	÷ 1000	1 – 11 k
.100 – 1.100 M	.1 – 1.1 M (FR6)	÷ 100	1 – 11 k
10.0 – 110.0 k	10 – 110 k (FR5)	÷ 10	1 – 11 k
1.00 – 11.00 k	1 – 11 k (FR4)	÷ 1	1 – 11 k
.100 – 1.100 k	.1 – 1.1 M (FR6)	÷ 100	1 – 11 k
10.0 – 110.0	10 – 110 k (FR5)	÷ 10	1 – 11 k
1.00 – 11.00	1 – 11 k (FR6)	÷ 100	1 – 11 k
.100 – 1.100	10 – 110 k (FR5)	÷ 10	1 – 11 k
10.0 – 110.0 m	1 – 11 k (FR4)	÷ 1	1 – 11 k

4.2.3.3 Frequency Counter

The frequency counter (ref: schematic 0103-00-1115 sheet 3) consists of a control flip flop (U6F) and four cascaded BCD ripple counters (U1A, U2A). This counter tallies the number of cycles from the prescalar over a 100 ms period. The output lines from the counter drive the frequency comparator.

When the GATE line goes high, the control flip flop (U6F) is enabled, allowing the counter to count until the GATE line goes low, inhibiting the control flip flop. Approximately 20 μs after the GATE line inhibits the flip flop, the CLRCNT line clears the flip flop and counter. When the GATE line returns high, the frequency counter again counts the frequency. For GATE and CLRCNT timing relationships, see figure 4-5.

4.2.3.4 Frequency Comparator

The frequency comparator (ref: schematic 0103-00-1115 sheet 3) serves two functions. First, it is part of the frequency display. Second, stabilizer enabled, it compares the input from the frequency counter with the stored frequency shown on the display. The resulting output at the

two latches (U1B, U3B) and two comparators (U2B, U4B) controls the frequency correction or sweep block.

Latches: The latch (U1B, U3B) receives its data directly from the frequency counter. The MEMCLK, when it goes high for 20 μs, clocks the frequency data to the output registers of the latches. Outputs from the latch drive both the display drivers and Q inputs of the frequency comparators (U2B, U4B). The MEMCLK occurs approximately every 100 ms, see figure 4-5 for timing relationships.

When the stabilizer is enabled, the MEMCLK line remains low. This holds the frequency data (displayed frequency) stored in the latches.

Frequency Comparator: The frequency comparator consists of two individual comparators (U2B, U4B) which are daisy chained together via gate U6C. It monitors data from the frequency counter and compares it against the outputs from the latches. This produces two levels which control the up/down counter in the frequency correction or sweep circuit.

When the stabilizer is off, the P and Q lines are always the same (P = Q). When the stabilizer is on, the P data can change while the Q data remains unchanged. The comparator detects the change and switches its two output lines (U4B pins 1 and 19) as shown in table 4-4.

Table 4-4. Comparator — U/D Counter Relationship

Condition	U4B Pin 19	U4B Pin 1	Correction U/D Counter
P = Q*	Low	High	Counter Disabled
P<Q	High	High	Counts Up
P>Q	High	Low	Counts Down

NOTE

P = Frequency data from the frequency counter.
Q = Frequency data from the latches.
*Also Stabilizer off condition.

4.2.3.5 Frequency Correction or Sweep.

When the stabilizer is on, the frequency correction circuit (ref: schematic 0103-00-1115 sheet 3), controlled by the frequency comparator, makes frequency corrections to the function generator loop. This block consists of the 8-bit up/down counter (U9F, U8F) and the DAC (U8G) along with its summing amplifier (U9G).

8-Bit Up/Down Counter: The 8-bit up/down counter (U9F, U8F), controlled by two lines from the frequency comparator, uses its output to increment or decrement the DAC. Table 4-4 illustrates how the comparator controls the up/down counter. The FRCHG pulse clocks the counter every 100 ms; see figure 4-5. The line SWPT from the mode control logic maintains the data inputs to the counter at a TTL low. When the stabilizer is turned on, the STAB line from the misc control logic goes high to enable the counter. For stabilizer off, the STAB line goes low and on the next FRCHG clock transition the outputs all go to a TTL low except the most significant bit which is held high. The 8 data lines from the counter directly drive the inputs of the frequency correction DAC.

Digital to Analog Converter and Summing Amplifier: The digital to analog converter (U8G), DAC, converts the 8 bits of digital data from the 8 bit up/down counter into a proportional analog current. The amplifier (U9G) sums the DACs current to produce a voltage which, when the stabilizer is on, drives the ASWP input of the function generator loop. A resistor (R29) sets the DAC's fixed reference DAC range is ±2% of the set frequency..

4.2.4 Output Block

The output block, shown in figure 4-6, consists of the square buffer, square selector, square shaper, sine converter, function select, preamplifier, output amplifier, and attenuator. It also has output protection circuits for both Func Out BNCs. The output block selects the appropriate waveform and connects it to the Func Out BNCs.

4.2.4.1 Square Buffer

The square buffer (ref: schematic 0103-00-1116 sheet 2) amplifies the square wave from the function generator loop (Q11 collector). The output (HFSQ) drives the trigger logic, frequency counter, and square selector. The square buffer is similar to the switch buffer (ref: paragraph 4.2.1.6) except for output phasing and output level. Square buffer output is 0 to + 5V. A highly differentiated portion of HFSQ is coupled through C24, C25 and C31 to the triangle node. This signal counteracts switching transients which are coupled through the current switch diode bridge.

4.2.4.2 Square Selector

The square selector (ref: schematic 0103-00-1116 sheet 3) picks either HFSQ from the square buffer or the low frequency square wave from the synthesizer. Outputs from the square selector drive the square shaper and Sync Out connector.

Above the 1.1 kHz frequency range, LF (U20 pin 13) is low, which enables U20 pin 4; the output (U21 pin 6) is the complement of HFSQ. This signal goes to U16 pin 2) and through two overvoltage protection inverters (U21) to the Sync Out connector.

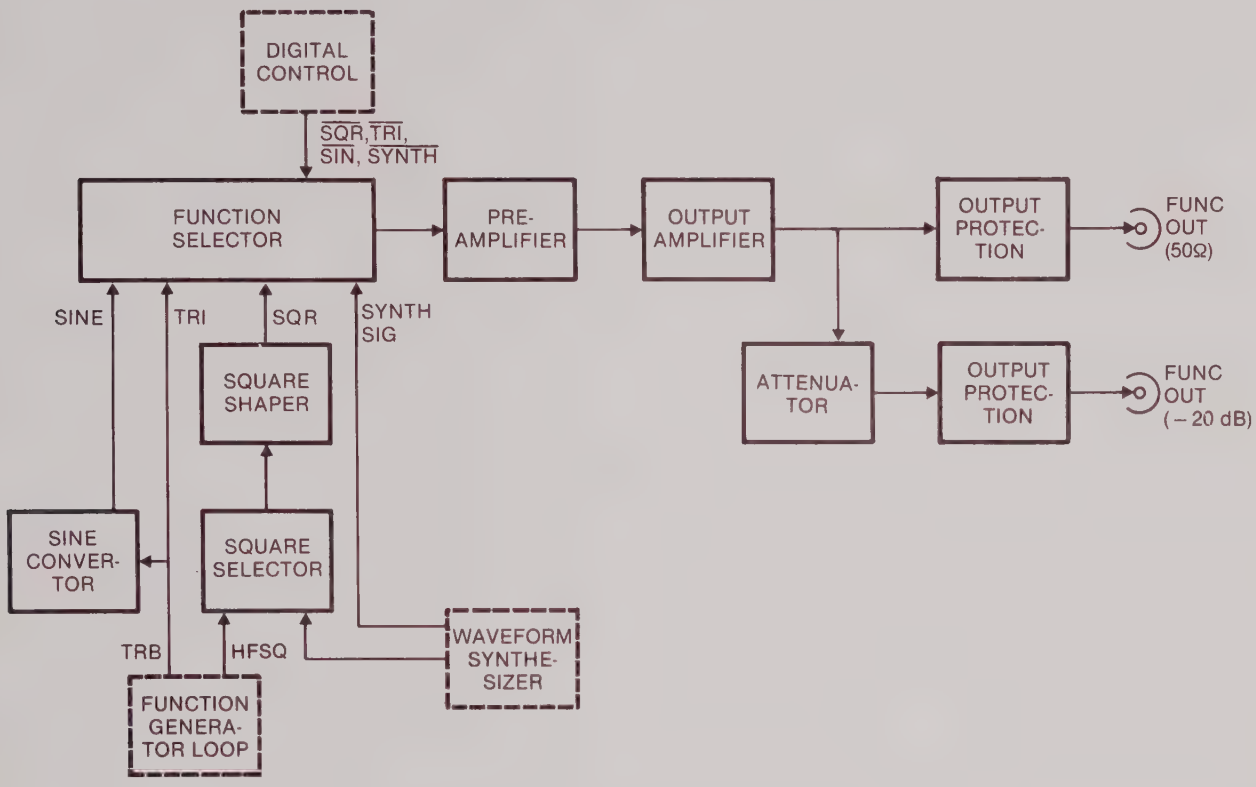


Figure 4-6. Output Block Diagram

For frequency ranges 1.1 kHz and below LF (U19 pin 9) is high, this enables U20 pin 3 and routes the square wave from the waveform synthesizer to U16 pin 2.

If Func is set to square wave, SQR at U19 pin 5 will be low, which puts U16 pin 1 high. The signal at U16 pin 2 will pass in phase to the square shaper via TTL SQ. For all functions other than square wave, SQR will be high disabling TTL SQ (U16 pin 12).

4.2.4.3 Square Shaper

The square shaper (ref: schematic 0103-00-1116 sheet 3) takes the TTL signal (TTL SQ) from the square selector and converts it to a clean, fast square wave current (± 1mA) that drives the preamplifier providing square wave is selected. The square wave is created by alternately sourcing and sinking current through the diode switch (CR36 through 39).

The voltage divider (R141, CR33, CR34, CR35, R144) converts TTL SQR to a bipolar signal, which switches the diodes in the square shaper. When TTL SQ is high, the voltage at the cathode of CR36 is approximately + 1.5V. CR38 sinks current from the TTL SQ signal while CR37 sources 1mA from the + 15V supply through U5 pin 6 to the preamplifier. When TTL SQ toggles low, the voltage at the cathode of CR36 is approximately – 1.5V. CR36 sources current to the TTL SQ signal and CR39 sinks 1mA from the preamplifier through U5 pin 6 to the – 15V supply. The current source and sink for upper and lower levels of square waves are independently adjustable by R142 and R147 respectively. Resistor R146 sets high frequency square wave peaking.

4.2.4.4 Sine Converter

The sine converter (ref: schematic 0103-00-1116 sheet 3) transforms the triangle into a sine wave for the function select. The sine converter uses the logarithmic response characteristics of the six matched diodes (U4) to approximate a sine wave current output. Buffered triangle output (TRB) enters the converter at U4 pins 2, 3, and 9. SIN DIST A trim pot (R121) adjusts the converter input for diode forward voltage variation. Two other adjustments, SIN DIST B and SIN DIST C (R132 and R137), balance the positive and negative peaks respectively. The current output is switched through FET switch

(U5) when $\overline{SIN}$ is low. TRI LEVEL trim pot (R126) adjusts the triangle form current that enters FET switch (U5) which is enabled by a low at $\overline{TRI}$.

4.2.4.5 Function Select

The function select circuit (ref: schematic 0103-00-1116 sheet 3) connects either the synthesizer output signal (SYNTH SIG), the square wave (TTL SQ), the sine converter output, or the buffered triangle (TRB) to the input of the preamplifier. Signal switching is handled by 4 section CMOS analog switch (U5). The synthesizer signal SYNTH SIG (U5 pin 14) is prevented from entering the preamplifier input (pin 15) until $\overline{SYNTH}$ goes low, which shorts pins 14 and 15 together. Switch bounce is prevented by C57 and C58 which eliminate ringing on the control line. Except for signal names and component numbers, the remaining 3 sections are identical and need no further discussion.

Both the triangle and sine FET switches (U5) are provided with increased isolation when they are not selected by shorting their inputs to ground through Q27 or Q28. For example, when $\overline{TRI}$ is high (not selected), Q26 is turned off, the collector of Q26 goes low, forward biasing Q27. This effectively shorts the emitter of Q27 together at ground.

4.2.4.6 Preamplifier

The preamplifier (ref: schematic 0103-00-1116 sheet 4) inverts and amplifies the signal current from the function selector to a sufficient voltage level for the output amplifier. The gain of the preamplifier is controlled by R184, which sets the sine wave amplitude. Zener diodes CR44 and CR45 convert the ±15V power supply voltages to ±9.4V.

4.2.4.7 Output Amplifier

The output amplifier (ref: schematic 0103-00-1116 sheet 4) provides the final gain and output drive capabilities of the instrument and is composed of an inverted summing amplifier (with a gain of about 10) for high-frequency signals, and a differential amplifier for dc and low-frequency signals. The differential amplifier also allows the dc offset of the Func Outputs.

AC Signal Path: High-frequency signals couple into the symmetrical emitter followers Q29 and Q32 through capacitors C91 and C92 respectively. These emitter followers drive the symmetrical inverter stage consisting of Q30 and Q33. Diodes CR46 and CR47, along with the 10Ω resistor R175, increase the switching speed of the output stage transistors Q31 and Q34 by maintaining a bias current which keeps them always partially on. The output signal (+ and − 20V, maximum) feeds back through resistors R176 and R177 to the input. Two 100Ω resistors (R196 and R197) set the output impedance for the Func Out (50Ω) connector.

DC Signal Path: The dc and low-frequency path in the output amplifier is through the transistor array (U26) connected as a differential amplifier. The output of the differential input stage (U26 pin 3), is inverted at U26 pin 9, and varies the current through transistor Q30. The signal at the collector of Q30 changes until the fed back signal through R176 and R177 balances with the input, either signals through R166 or offset through R167 and R168. The PNP transistors (U26) balance the current through the differential input pair and provide a high impedance load for the first stage output. Capacitor C85 limits the speed of this section at high frequencies.

Offset Circuit: When the D.C. Offset switch is turned on, the voltage on the wiper of R3 is converted to current through R167 and R168. This current is proportional to the voltage and polarity at the wiper of R3 and enters the summing node to provide dc control of the input current, and therefore the output voltage offset.

4.2.4.8 Attenuator

The attenuator (ref: schematic 0103-00-1116 sheet 4), consists of a 498Ω resistors (R198 and R199) and a 54.9Ω resistor (R200), provides 20dB of attenuation at 50Ω output impedance to the Func Out (−20dB) connector.

4.2.4.9 Output Protection

The output protection circuits (ref: schematic 0103-00-1116 sheet 4) guard the output amplifier from excessive external voltages that could be accidentally connected to either of the Func Out BNCs that could damage the instrument.

There are two safeguards to protect the output amplifier.

1. Two in-line fast-blow fuses for each Func Out connector.
2. Four voltage-limiting, high current diodes (CR50 through CR53) that provide additional protection at the Func Out (50Ω) connector.

4.2.5 Pushbutton Interface

When a front panel pushbutton is pressed, one of the inputs to the pushbutton interface (ref: figure 4-7 and schematics 0103-00-1115 sheet 1 and 0103-00-1117) is connected to either +5V or ground reversing the logic level of the appropriate pushbutton interface output. The MAN TRIG line from the pushbutton interface goes to the trigger logic, while the remaining lines go to the digital control block. Each switch drives a Schmitt trigger gate. RC circuits prevent multiple pulsing at the input of each gate. Outputs drive the appropriate control circuit within the unit.

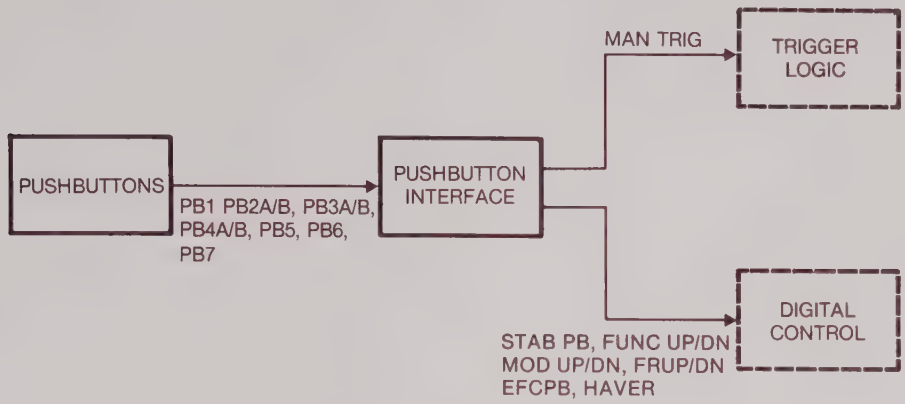


Figure 4-7. Pushbutton Interface

4.2.6 Digital Control

The digital control block (figure 4-8) consists of the power on reset, mode control, misc. control, frequency range control and function control circuits.

4.2.6.1 Power-On Reset

The power-on reset circuit (ref: schematic 0103-00-1115 sheet 3) sets all other digital control block circuits to an initial state. On initial power up, C57 holds U3G pin 13

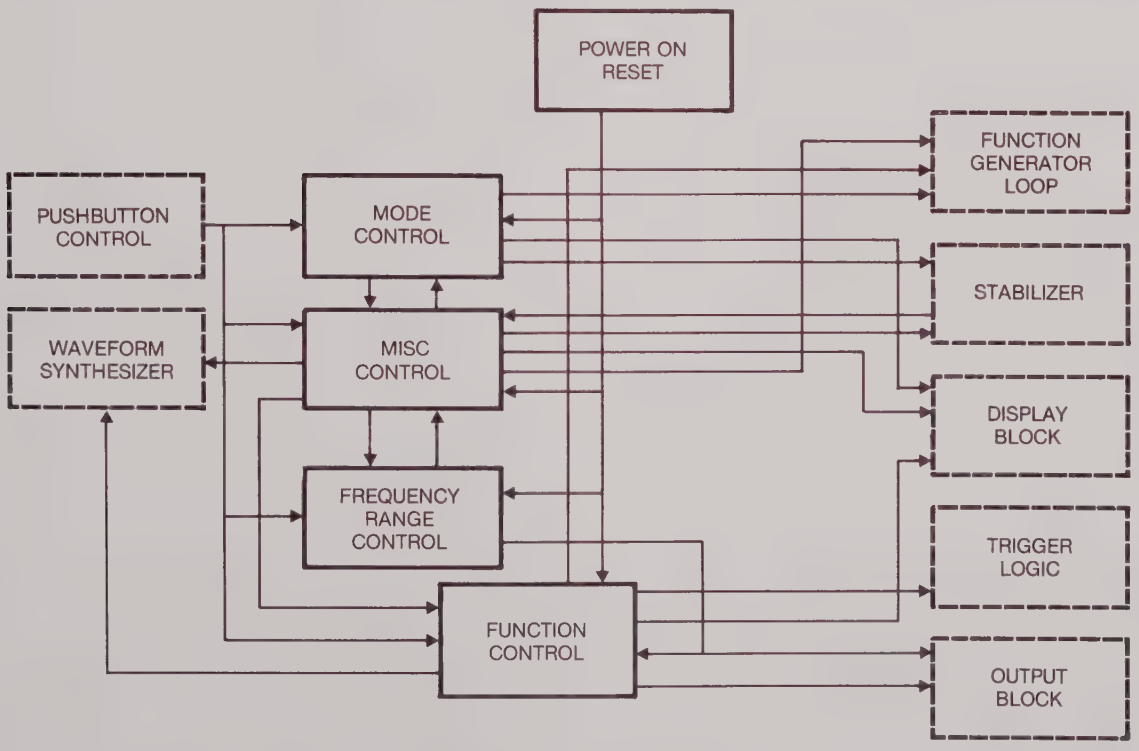


Figure 4-8. Digital Control

low, MR (U3G pin 12) goes high, and $\overline{MR}$ (U3G pin 4) goes low; MR and $\overline{MR}$ reset the various digital control circuits. After about ½ second, C57 charges to approximately 2.5V, pin 12 (MR) toggles low, and pin 4 ($\overline{MR}$) toggles high. These levels now remain constant for the remainder of the time the unit is on.

4.2.6.2 Mode Control

As the Mode pushbutton control lines (ref: figure 4-9) are pulsed, the mode control circuit steps through a sequence of modes either up (MOD UP) or down (MOD DN). This selects one of the output mode lines low. These mode lines, in conjunction with additional logic gates, control the trigger logic, stabilizer, display block, and misc control. External frequency control ($\overline{EFC}$) combines with $\overline{CONT}$ and $\overline{STOP}$ to produce BL.

The mode control circuit (ref: schematic 0103-00-1115 sheet 2) contains the up/down counter (U4G), which has separate "count up" and "count down" inputs, and receives pulsed signals from U5G originating from the MOD UP and MOD DN pushbutton buffers. The output of this counter drives decoder U4F, which selects one of the available modes. The two NAND gates (U5G) serve to prevent any fruther up or down count beyond the capability of the unit. At one extreme (Cont Mode), U5G pin 8 is low, causing pin 10 to remain high at all times, disabling pin 9. In the other extreme, (Gate Mode), U5G pins 11, 12, and 13 perform the same function. The lines $\overline{SWPT}$ and $\overline{SWP}$ always reamins low, while the line $\overline{SWP}$ always remains high. MC0 and MC1 control the trigger logic. $\overline{CONT}$ controls the misc. control. $\overline{GATE}$, $\overline{TRIG}$, and $\overline{CONT}$ enable the appropriate segment on the front panel display. In Trig or Gate Modes, BL disables all number segments of the display.

4.2.6.3 Misc Control

The misc control circuit (ref: figure 4-10 and schematic 0103-00-1115 sheet 2) performs various functions within the instrument. Its circuits selects the internal or external references, enables or disables the haverwaves, and turns on or off the stabilizer.

Internal/External Reference: The reference counter (U8C) receives a pulse from the pushbutton interface circuit (U3G pins 10 and 11) each time the Ref pushbutton is pressed. This causes the counter output (U8C pin 3) to change states. The output (EFC) turns on and off the Ext Ref annunicator. The inverter (U8D) inverts the EFC input to produce $\overline{EFC}$ which blanks the display (BL), selects the reference source, turns on and off the Int Ref annunciator, and selects the synthesized waveform.

Haverwave: The haver wave counter (U7A) receives a pulse from the pushbutton interface (U3G pin 6) each time the Haver pushbutton is pressed. This causes the counter output (U7A pin 3) to change states. To enable the haver wave, both the counter output and the line LF must be high which causes lines THAV and CHAV to be high. THAV controls the trigger logic circuit and CHAV enables the Hav annunciators. LF is high when external reference is selected or the synthesized frequency ranges are selected or both.

Stabilizer: The stab flip-flop (U6F) receives a pulse (STABPB) from the Pushbutton Interface. Since both J/K inputs to U6F (pins 10 and 11) are always high, the two flip-flop outputs (pins 14 and 15) change state each time the flip-flop receives a STABPB pulse. When the stabilizer is off, STAB is high. U4E inverts $\overline{STAB}$ to produce STAB which, when low, MEMCLK is pulsed with each transition of U7E pin 13. When the stabilizer is on, $\overline{STAB}$ is low, making STAB high, which in turn holds MEMCLK low at all times. With $\overline{STAB}$ low, VCG KILL is high, disconnecting the VCG In BNC from the input of the VCG circuit. The stabilizer is disabled by U6G pin 1 if UNSTAB (U6G pin 3) goes low, caused by the freq going out of range, or if the unit is in any mode other than Cont.

4.2.6.4 Frequency Range Control

The frequency range control circuit (ref: figure 4-11 and schematic 0103-00-1115 sheet 2) steps through a sequence of frequency ranges. As the Freq Range pushbutton is pressed, the pushbutton interface detects whether the frequency range should increase (FRUP) or decrease (FRDN). The circuit's output lines control the stabilizer, display block, output block, function control, and misc control. External frequency control ($\overline{EFC}$) combines with other control lines to produce LF.

Up/down counter (U6E), which has separate "count up" and "count down" inputs, receives pulsed signals from U5F originating from the freq range (FRUP and FRDN) pushbutton buffers. The output of this counter drives decoder (U6D), which selects one of its output lines to be low. $\overline{FR7}$, which controls the HF COMP on the analog board and goes to the frequency counter, is driven directly by one of these lines. From the remaining output lines are decoded the appropriate frequency range control lines (FR4, FR5, and FR6), which are inverted by the frequency counter circuit before going to the analog portion of the generator. The 9 output frequency ranges of the generator originate from these 4 control lines (FR4, FR5, FR6, and $\overline{FR7}$), the low frequency synthesizer, and the ÷ 100 control line. In the 5 lowest ranges, LF is high which, unless square function is selected, enables $\overline{SYNTH}$ (through the function control). This connects the output of the LF waveform synthesizer to the input of the preamplifier. The output frequency of the synthesizer is 1/1000th of the range selected. For example, if FR5

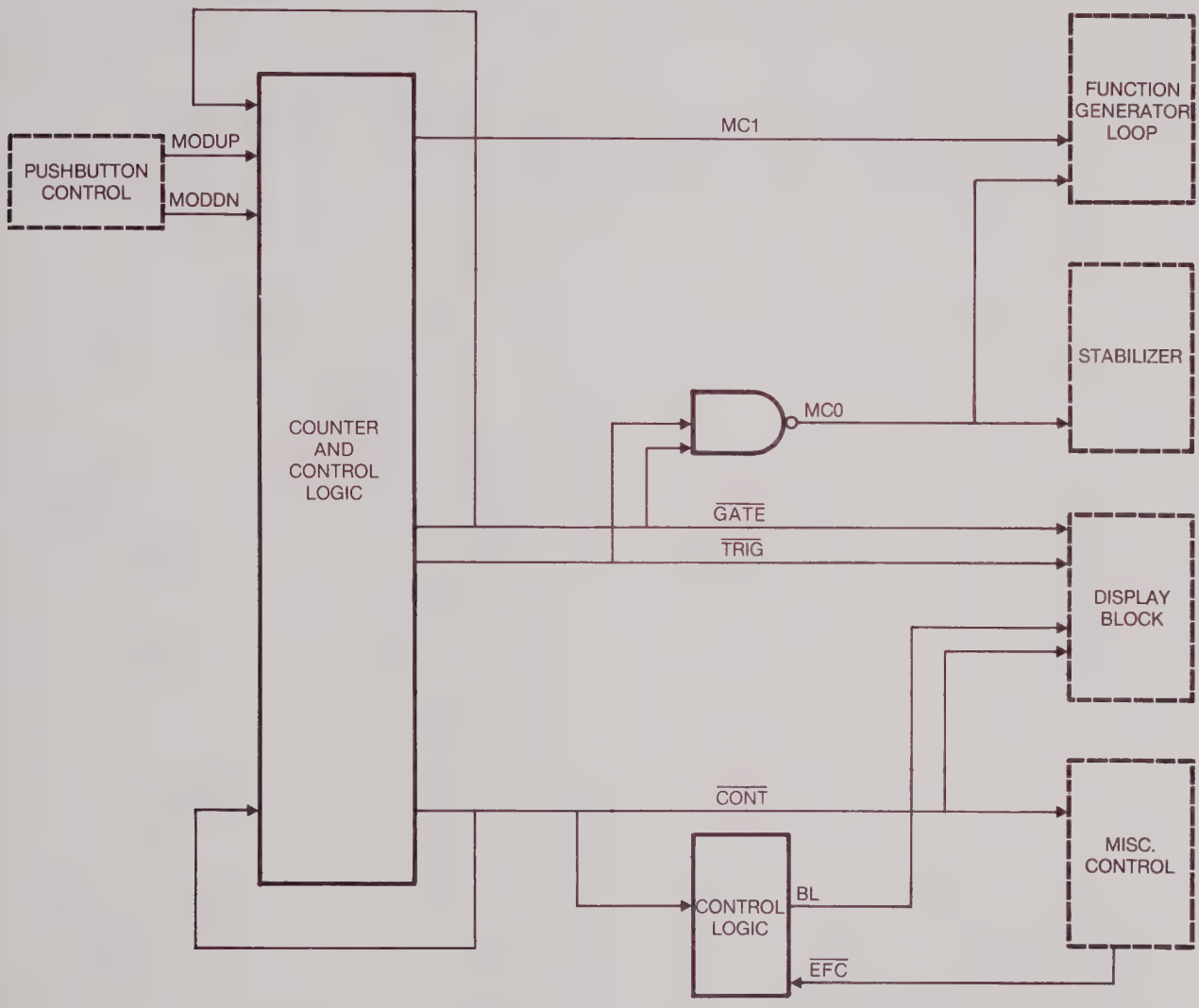


Figure 4-9. Mode Control

(110kHz range) is selected, the output frequency range of the synthesizer (and therefore the Func Out connectors), would be 110Hz. In addition, in the 3 lowest ranges, $\overline{\div 100}$ is low, further dividing this signal by 100. Using the same example, the synthesizer output frequency range would now be 110 mHz. Two NAND gates (U5F), serve to prevent any up or down count beyond the capability of the unit. At one extreme (110mHz frequency range), U5F pin 1 is low, causing pin 3 to remain high at all times, disabling pin 2. In the other extreme, (11.00 MHz), U5F pins 8, 9, and 10 perform this function. On the display, DmHz controls the "mHz" emblem, DHz controls "Hz", DK controls "K", and DMHz controls "MHz". The decimal points are controlled by DDP1, DDP2, and $\overline{\text{DDP3}}$.

4.2.6.5 Function Control

The function control (ref: figure 4-12 and schematic 0103-00-1115 sheet 2), steps through a sequence of functions. As the Func pushbutton is pressed, the Pushbutton Interface detects whether the function should increase (FUNCUP) or decrease (FUNCDN). The

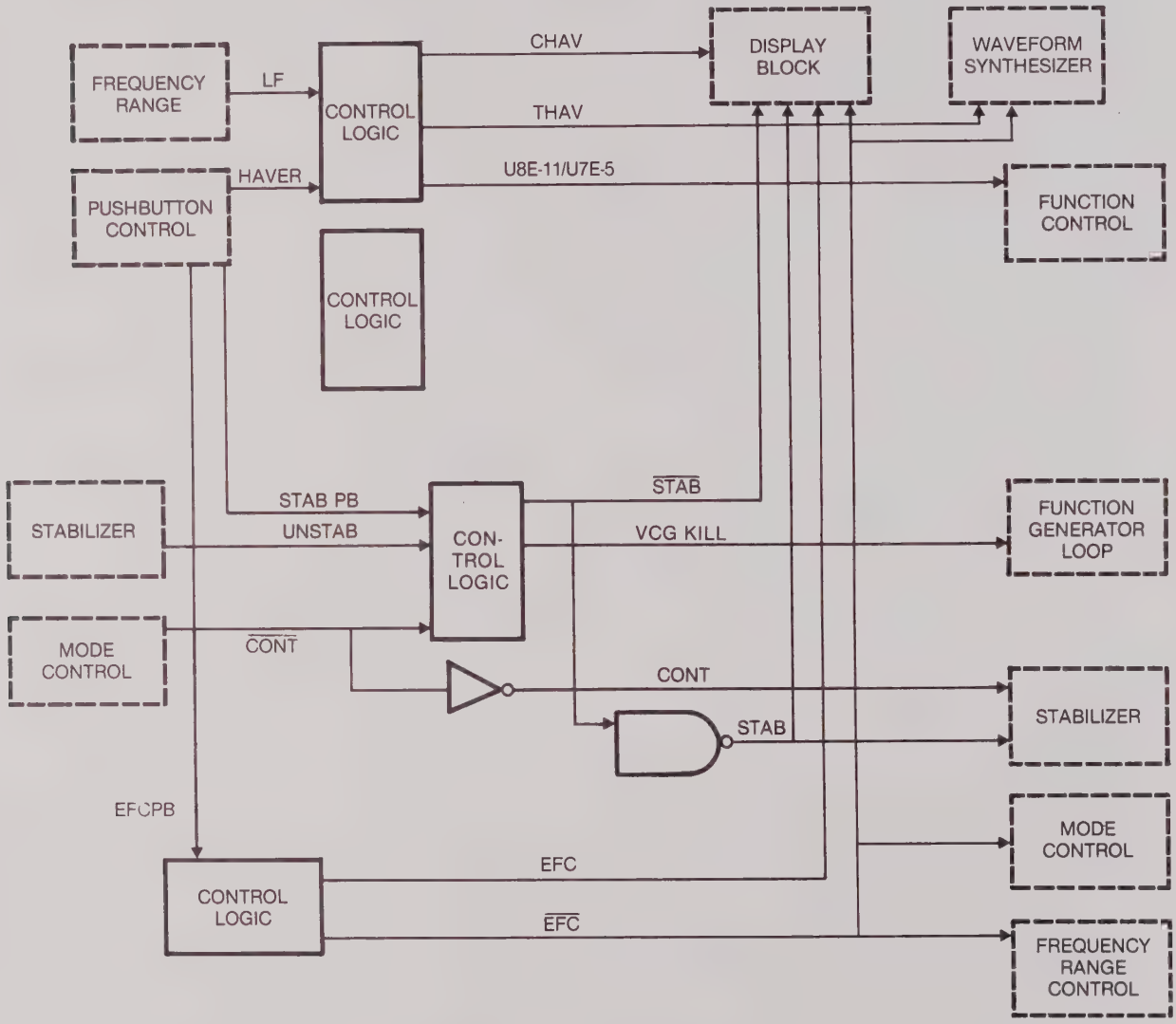


Figure 4-10. Misc Control

circuits output lines control the waveform synthesizer, display block, output block, and trigger logic.

Up/down counter U5D, which has separate "count up" and "count down" inputs, receives pulsed signal from U5F originating from the FUNC UP and FUNC DN pushbutton buffers. The output of this counter drives decoder U4D, which selects one of the available functions. The two NAND gates (U5F) serve to prevent any further up or down count beyond the capability of the unit. At one extreme (DC), U5F pin 13 is low, which causes pin 11 to remain high at all times and disables pin 12. In the other extreme, (negative going ramp), U5F pins 4, 5, and 6 perform the same function. In the nonsynthesized frequency ranges, output lines $\overline{TRI}$, $\overline{SIN}$, and $\overline{SQR}$ select the waveform to be sent to the preamplifier. When LF (from the frequency range control circuit) is high and the unit is in sine, triangle, or either ramp function, $\overline{SYNTH}$ is low which connects the output of the LF waveform synthesizer to the input of the preamplifier. FS0 and FS1 select the waveform at the LF waveform synthesizer output. When the unit is in square function, $\overline{SQR}$ is low, which connects the output of the Square Shaper to the input of the preamplifier. $\overline{\sim}$, $\overline{\sqcup}$, $\overline{\sim}$, $\overline{\diagdown}$, $\diagup$ enable the appropriate segment on the front panel display.

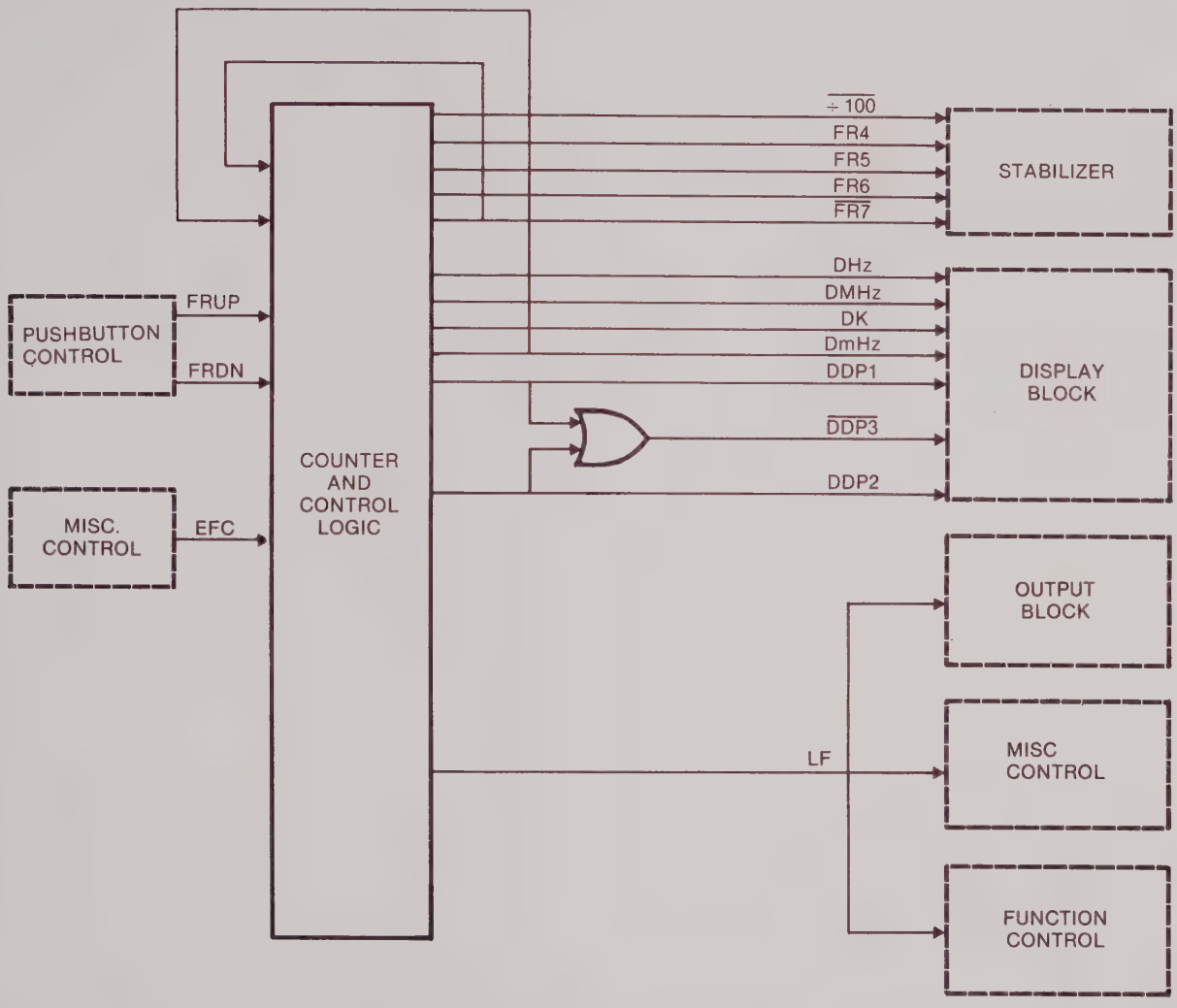


Figure 4-11. Frequency Range Control

4.2.7 Display Block

The display block (ref: figure 4-13 and schematics 0103-00-1115 sheet 1 and 0103-00-1117) consists of the display drivers and the display. Two 30 Hz signals, (BP and its complement $\overline{BP}$) originating from U5C, synchronize the LCD and the segment drivers. To enable a segment of the display, 5Vrms is needed between BP and the control line for that segment. Therefore, BP and the segment control line must be out of phase from each other.

The following example explains all exclusive-or gates which drive the bars, arrows, and decimal points on the display. When the unit is in Cont Mode, U3F pin 9 ($\overline{CONT}$) is low. The $\overline{BP}$ signal at pin 8 is in phase with the signal at pin 10 (Z3) and is therefore out of phase with BP. This results in a rms voltage of 5V between BP and Z3, enabling the segment. When the unit is not in Cont Mode, a high at pin 9 causes the output at pin 10 to be in phase with BP, resulting in an rms voltage of 0V, disabling the segment. Data for these gates originate from the various digital control circuits in the unit.

Lines D2A through D4D, which originate from the frequency comparator, determine which number segments are enabled. Each output line (2A through 4G) drives a

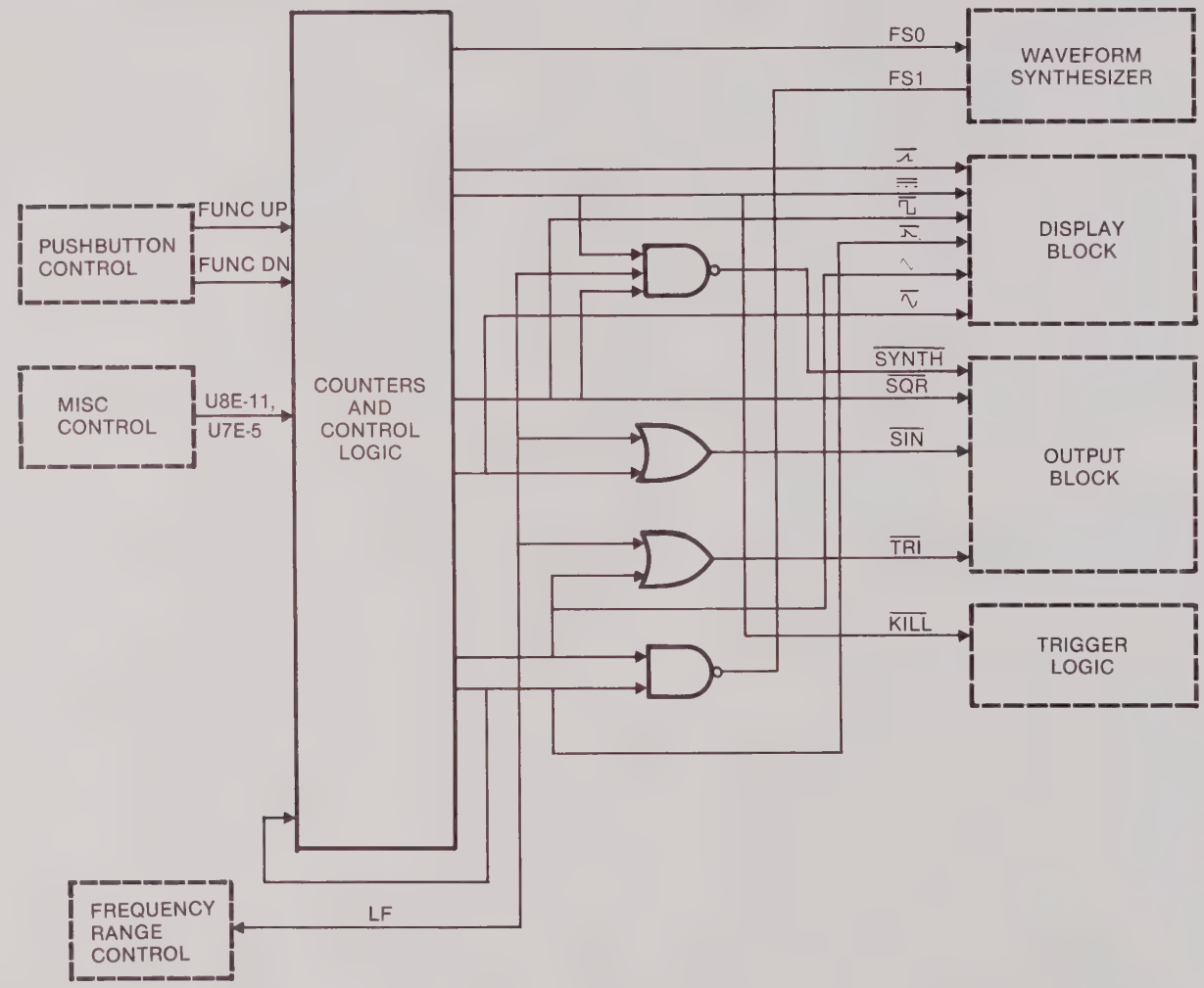


Figure 4-12. Function Control

number segment except in Trig or Gate Modes when they are disabled by BL.

4.2.8 Power Supply

Three power supply voltages, +15V, −15V, and +5V are generated on the power supply circuit board (ref: schematic 0103-00-1113).

4.2.8.1 +5V Supply

In the +5V supply, ac from the transformer T1 (located on the rear panel), is rectified by CR2 and filtered by C9, C10, and C11 to provide unregulated dc for regulator VR2. This three-terminal regulator normally operates with a 1.25V difference between its input and output terminals. C12 provides additional filtering at the output of the regulator.

4.2.8.2 ±15V Power Supplies

The ±15V Power Supplies provide power to the analog sections of the instrument. R2, which is in series with the output of the +15V regulator, causes current limiting to take place at a lower value than the internal limiting provided by the regulator. As the current through R2 reaches its limiting value, the voltage drop across R2 reaches 0.4V. Any further current through R2 causes the regulator to lower the output voltage until the current falls back to the limiting value.

The −15V supply operates similarly to the +15V supply, however the polarities are reversed.

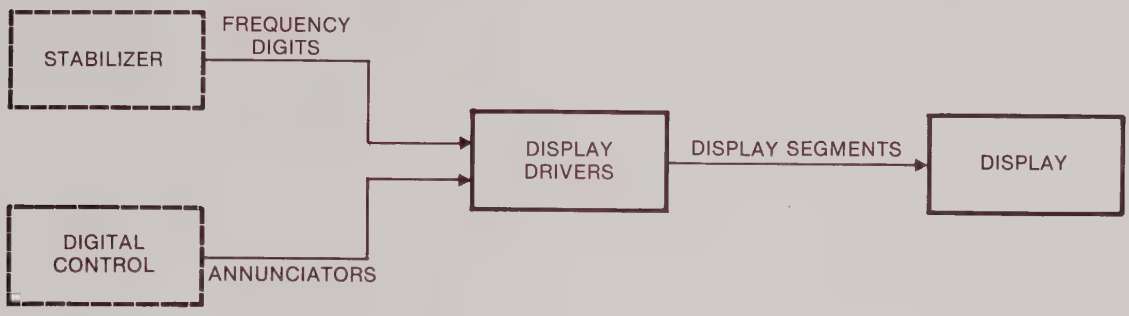


Figure 4-13. Display Block

SECTION 5
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

5.2 REQUIRED TEST EQUIPMENT

Voltmeter	Millivolt dc measurement (0.1% accuracy), true rms
Oscilloscope, Dual Channel	≥100 MHz bandwidth
Counter	≥20 MHz (0.01% accuracy)
50Ω Feedthru	±0.5% accuracy, 2W
Distortion Analyzer	To 200 kHz
RG58U Coax Cable	3 ft length BNC male contacts
Spectrum Analyzer	To 60 MHz

5.3 CALIBRATION

NOTE

Before removing the cover, disconnect the instrument from the ac power source. Refer to Section 2 for cover removal, except leave top cover on and remove only bottom cover for calibration. Invert the instrument so generator board adjustments are on top and place the bottom cover on top of the unit to maintain the operating temperture during calibration.

After referring to the following preliminary data, perform calibration, as necessary, per table 5-1. If performing partial calibration, check previous settings and adjustments for applicability. Figure 5-1 shows waveform generator board calibration points.

NOTE

The completion of these calibration procedures returns the instrument to correct calibration. All limits and tolerances given in these procedures are calibration guides and should not be interpreted as instrument specifications. Instrument specifications are given in Section 1 of this manual.

1. All measurements made at the FUNC OUT connector must be terminated into a 50Ω (±0.5%) load.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

2. Start the calibration by removing the bottom cover, connecting the unit to an ac source, and setting these front panel switches as follows:

Frequency	
Fine	cw
Coarse	cw
Amplitude	cw
D.C. Offset	Off

3. Allow the unit to warm up at least 30 minutes for final calibration. Keep the instrument covers on to maintain heat. Lift bottom cover only to make adjustments or measurements.

Table 5-1. Calibration Procedure

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
1	Power Supply Regulators	DC Voltmeter	J10 Pin 2	Paragraph 5.3 step 2			Black (−) lead ground
2			J10 Pin 5			−15V ± 350 mV	Red (+) lead dc volts
3			J10 Pin 6			+5V ± 250 mV	
4			J10 Pin 7			+15V ± 350 mV	
5	Triangle Amplifier Balance		J10 Pin 3		R103	0V ± 100 mV	Rough adjustment only
6					R86	0V ± 20 mV	
7	Function Out	Scope	Func Out (50Ω)			10Vp-p sine wave (Approximately 2 cycles)	Terminate with 50Ω Scope Settings: 2V/div. 0.2ms/div.
8				Step Func button to right		Functions match display (correct amplitude and frequency)	
9	Output Amplifier Balance			Func: ⎓ (dc)	R157	0V ± 10 mV	Display shows 00.0 kHz Scope setting: 10 mV/div. (or maximum scope sensitivity if more than 10 mV)
10	Trigger Baseline			Freq range: step to right twice to 110.0 kHz range Func: ∿ Mode: Trig	R103	0Vdc ± 50 mV	Scope setting: 0.1V/div. Verify baseline 0VDC ± 100 mV over full range of Coarse Frequency knob (Frequency Fine knob full cw)
11	VCG Zero	DC Voltmeter	VCG In BNC	MODE: CONT Func: ⊓ Frequency knobs: both fully ccw	R11	0V ± 0.5 mV	Use coax cable with no termination
12	1100:1 Frequency	Scope	Func Out (50Ω)		R13	First transition occurs at center vertical grid line, for 50 Hz.	Use coax cable with 50Ω termination Scope settings: 2V/div. 2ms/div. Trigger slope: − (Neg) Horizontal position: Trace begins at extreme left vertical grid line
13	1100:1 Symmetry				R38	Second transition occurs at extreme right vertical grid (within 2% (1 minor division)	Repeat steps 12 and 13 if necessary. Alternate method: magnify X10 and alternate trigger slope between + and −, set R38 for <2 divisions assymetry.
14	High Symmetry			Frequency knobs: fully cw Freq Range: 11.00 kHz	R20	<0.1% (½ minor div.) symmetry	Scope setting: 2V/div. 10μs/div. X10 Magnification, alternate trigger slopes while adjusting R20 for minimum assymetry.

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
15		Scope	Func Out (50Ω)	Coarse Frequency: 5kHz	Verify only	<0.5% asymmetry (Verify <2½ minor divisions)	Scope setting: 20μs/div. Magnification: Off
16	Sine Distortion	Distortion Analyzer		Frequency knobs: fully cw Func: ∿	R121, R132, R137, R86	Minimum distortion (typically 0.2 to 0.3%)	Adjust R86 slightly if necessary.
17	Full Scale Frequency	Counter		Func: ⊓	R1	11.15 kHz on display	Display reads same as counter ± 0.01 kHz
18		Display		Switch between Range: 11 kHz and 110 kHz Freq Ranges		11 kHz Freq Range: 11.05 kHz to 11.25 kHz. 110 kHz Freq Range: 110.5 kHz to 112.5 kHz.	Set for best frequency balance between freq ranges. C44 (.001 μF nominal value) trims 11.00 kHz range.
19	11:1 Frequency			Freq Range: 110 kHz Frequency Coarse knob: fully ccw	Verify only	10 kHz ± 2 kHz on display	
20	High Frequency Calibration			Frequency knobs: fully cw Freq Range: 1.100 MHz	C40	1.115 MHz ± .005 MHz on display	C41 may be trimmed to obtain equal adjustment above and below 1.110 MHz
21				Frequency Coarse knob: fully ccw		Note display reading	
22				Freq Range: 11.00 MHz Frequency Coarse knob: fully ccw	C38	Set for 10 times reading noted in previous step	C39 may be trimmed to obtain equal adjustment above and below goal frequency
23				Frequency knobs: fully cw	R80	11.15 MHz ± .05 MHz	
24	Amplitude	True rms Voltmeter		Func: ∿ Freq Range: 11.00 kHz Freq Coarse Knob: fully ccw	R184	3.55 Vac ± 0.015 Vac (3.535 Vac to 3.565 Vac)	
25				Func: ∿	R126	2.90 Vac ± 0.015 Vac (2.885 Vac to 2.915 Vac)	
26				Frequency knobs: fully cw Freq Range: 1.100 kHz	R151		

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
27	Amplitude	DC Voltmeter	Func Out (50Ω)	Freq Range: 110.0 mHz Function: ⊓⊔	R142	+5.025 Vdc ± 0.025 Vdc +5.00 Vdc to 5.05 Vdc on positive peak	Turn frequency coarse knob fully ccw to hold each peak while adjusting, then return cw
28					R147	−5.025 Vdc ± 0.025 Vdc −5.00 Vdc to −5.05 Vdc on negative peak	
29	Waveform Quality and Frequency Response	Scope		Frequency knobs: fully cw Freq Range: 1.100 MHz Amplitude: 8Vp-p	R146	Minimum aberations <4% (320 mV)	Scope settings: 2V/div. 0.1 μs/div. (Observe peak-to-peak aberations at 0.5V/DIV by adjusting vertical position)
30				Amplitude: fully cw		Rise/Fall <22 ns	Scope settings: X10 Magnification
31				Func: ∿ Frequency knobs: fully cw Freq Range: 11.00 MHz	Verify only	Amplitude between 8.6V and 10V inclusive	Scope settings: Magnification Off
32		Spectrum Analyzer		Freq Range: 1.100 MHz		Harmonics less than −40 dBc from 1.1 MHz to 0.1 MHz	Rotate coarse freq control through its range and return fully cw
33				Freq Range: 11 MHz		Harmonics less than −28 dBc from 11 MHz to 1 MHz	
34	D.C. Offset	Scope or DC Voltmeter		Function: ⎓ (dc) D.C. Offset: fully cw		Minimum +5VDC	Calibration complete, start of functional check out.
35				D.C. Offset: ccw (not in detent)		−5VDC or more negative	
36	−20 dB Output	Scope		D.C. Offset: Off Func: ⊓⊔ Frequency knobs: fully cw Freq Range: 11.00 kHz		Approximately 10Vp-p square wave	Scope settings: 2V/div. 20μs/div.
37			Func Out (−20 dB)			Approximately 1Vp-p square wave. Note value.	Scope settings: .2V/div.
38			Func Out (50Ω)	Amplitude: fully ccw		Verify Vp-p less than value noted in step 37	

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
39	Sync Out	Scope	Sync Out	Amplitude: fully cw	Verify only	Normal TTL level square wave	Remove 50Ω termination Scope setting: 2V/div.
40	Trigger, Gate and Haver			Mode: Trig		Display shows Trig (numbers blanked)	Approximately 0Vdc
41			Func Out (50Ω)	Func: ∿		Verify triggered sine wave	Connect 1kHz TTL signal from external source to channel 2 and Trig In (TTL) BNC. Scope settings: .2ms/div. Trigger to channel 2 Monitor channel 1
42				Mode: Gate		Display shows Gate Verify gated sine wave	
43				Freq Range: 1.100 kHz Haver: On		Gated Haversine	Change external signal at Trig In (TTL) BNC to 100 Hz Scope settings: 2ms/div.
44	Manual Trigger			Haver: Off		Sine wave when Trigger button pressed	Disconnect external signal source, scope channel 2 and Trig In (TTL) Trigger to channel 1
45	VCG In			Mode: Cont Freq Range: 110.0 kHz Frequency knobs: fully ccw Func: ⊓		Display shows 110 kHz ± 5 kHz	Connect +5VDC to VCG In BNC. Verify STAB is off.
46						Verify one cycle >5 divisions	Remove voltage from VCG In BNC Scope setting: 2ms/div.
47	External Reference			Frequency knobs: fully cw Freq Range: 1.100 kHz Func: ∿ Ref: Int		Waveform changes to DC at various voltage levels as Ref In (TTL) BNC intermittently shorted to ground	Scope setting: .2ms/div.
48				Ref: Ext		Slightly over 2 cycles displayed on scope. Instrument display blanked	Connect 1.1 MHz TTL signal to Ref In (TTL) BNC

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
49	Stab	Scope	Func Out (50Ω)	Stab: Off Ref: Int Frequency Fine: initially centered Frequency Coarse: adjust for 500Hz Func: ⊓⊔ Stab: On	Verify only	Quickly turn Frequency Fine knob as indicated and verify the following: 1) Rotate fine control cw to move transition from center to 3 cm 2) Transition travels approximately 2 centimeters toward center of scope display 3) Transition jumps back to 3 centimeters left of center grid line 4) Stab now Off	Disconnect Ref In BNC Scope settings: X10 Magnification: On Adjust horizontal position for square wave transition at center vertical grid line Stab automatically disengages when it reaches its electrical limit.
50				Use Frequency Fine knob to return square wave transition to center vertical grid line Stab: On		Same as step 49 in opposite direction	Repeat as in step 49 except turn Frequency Fine knob ccw to initially move transition 3 centimeters right
51	Frequency Ranges			Frequency knobs: fully cw		Display reads between 1.105 kHz and 1.125 kHz.	Scope settings: 50μs/div. X10 Magnification: Off Set horizontal variable for 1 cycle on screen
52				Freq Range: 110.0 Hz		Display reads between 110.5 Hz and 112.5 Hz. Scope screen shows 1 cycle.	Scope setting: 0.5ms/div.
53				Freq Range: 11.00 Hz		Display reads between 11.05 Hz and 11.25 Hz. Scope screen shows 1 cycle.	Scope setting: 5ms/div. Trigger mode: Normal
54				Freq Range: 1.100 Hz		Display reads between 1.105 Hz and 1.125 Hz. Scope screen shows 1 cycle.	Scope setting: 50ms/div.
55				Freq Range: 110.0 mHz		Display reads between 110.5 mHz and 112.5 Hz. Scope screen shows 1 cycle.	Scope setting: 0.5 sec/div.

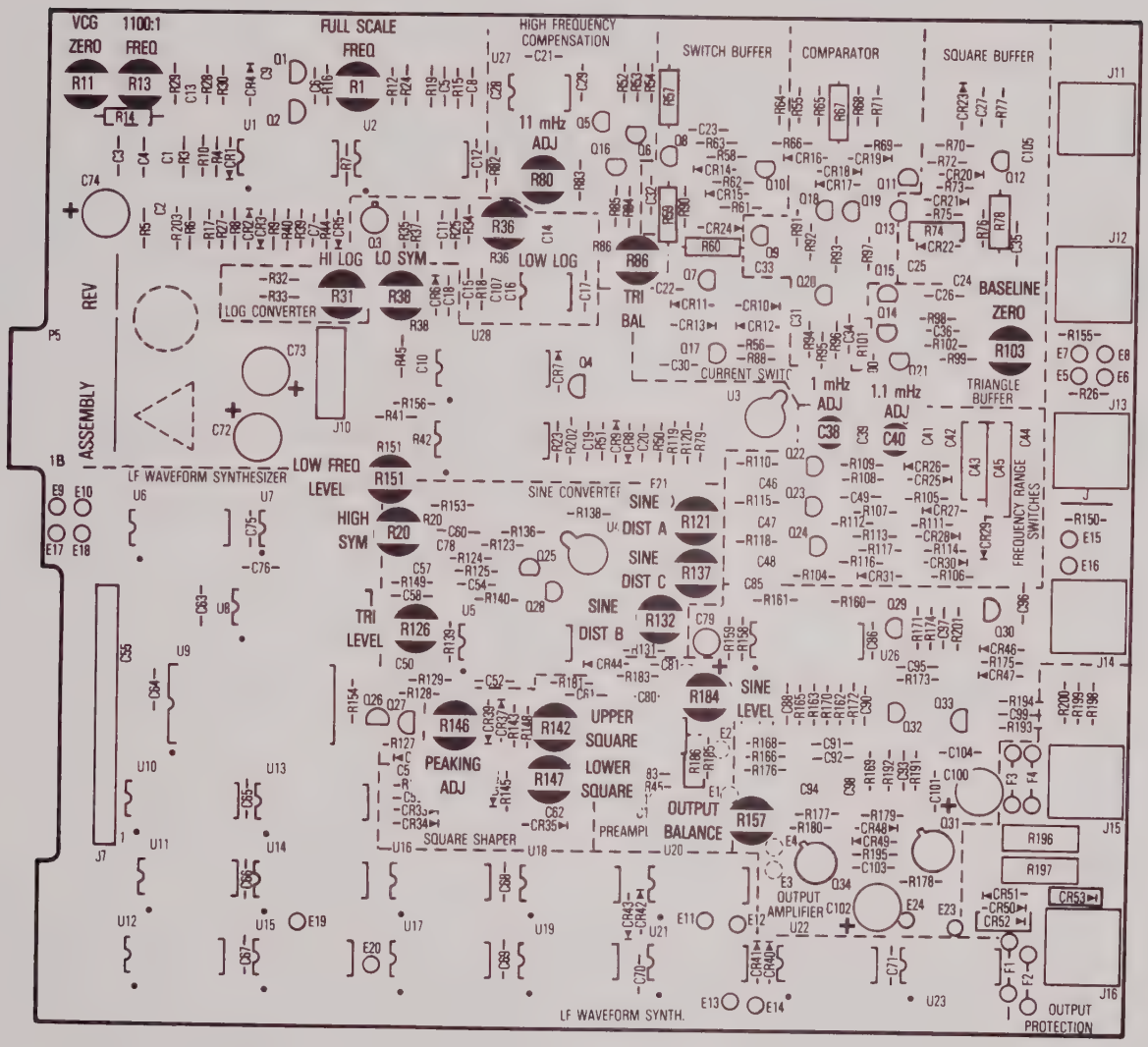


Figure 5-1. Calibration Points

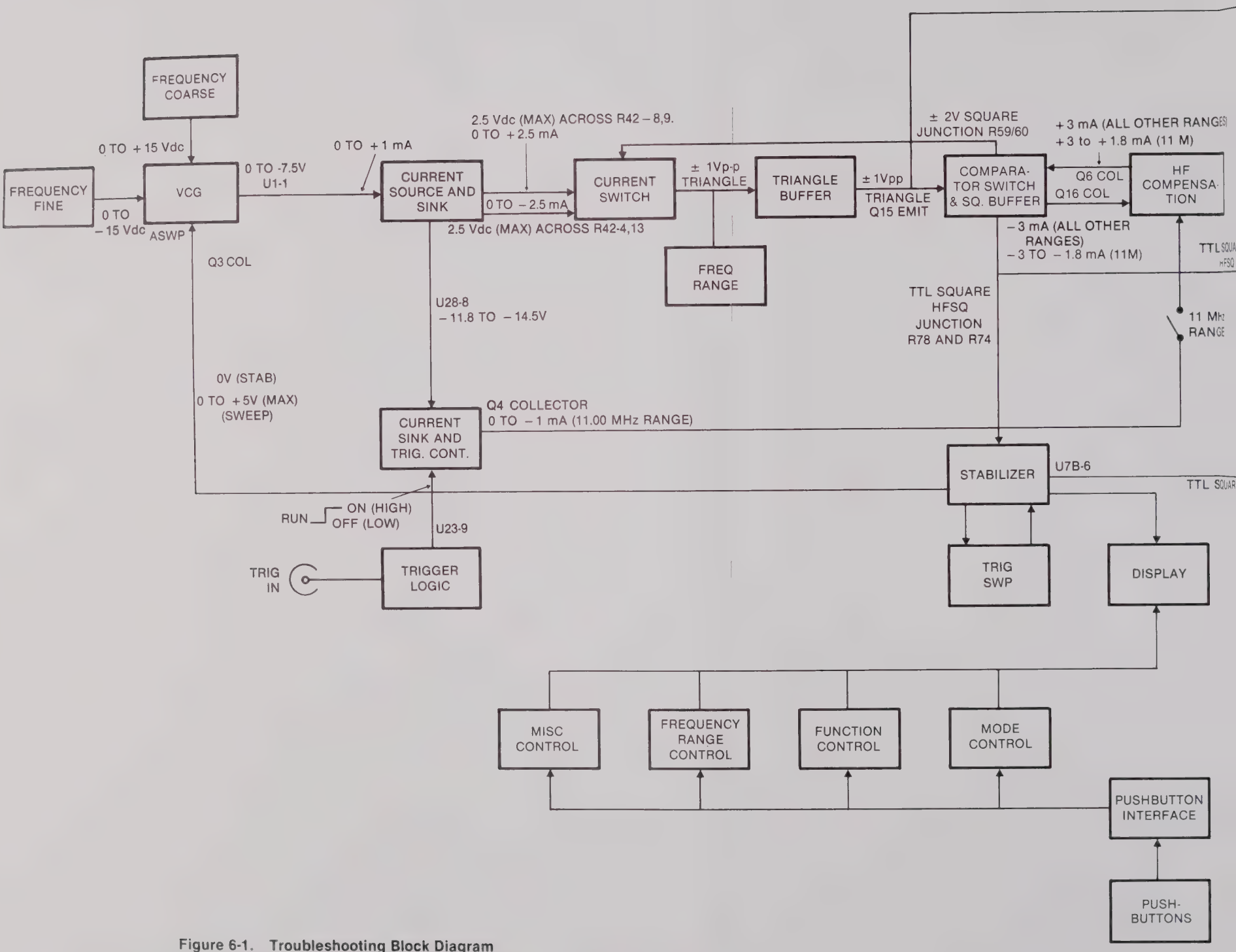
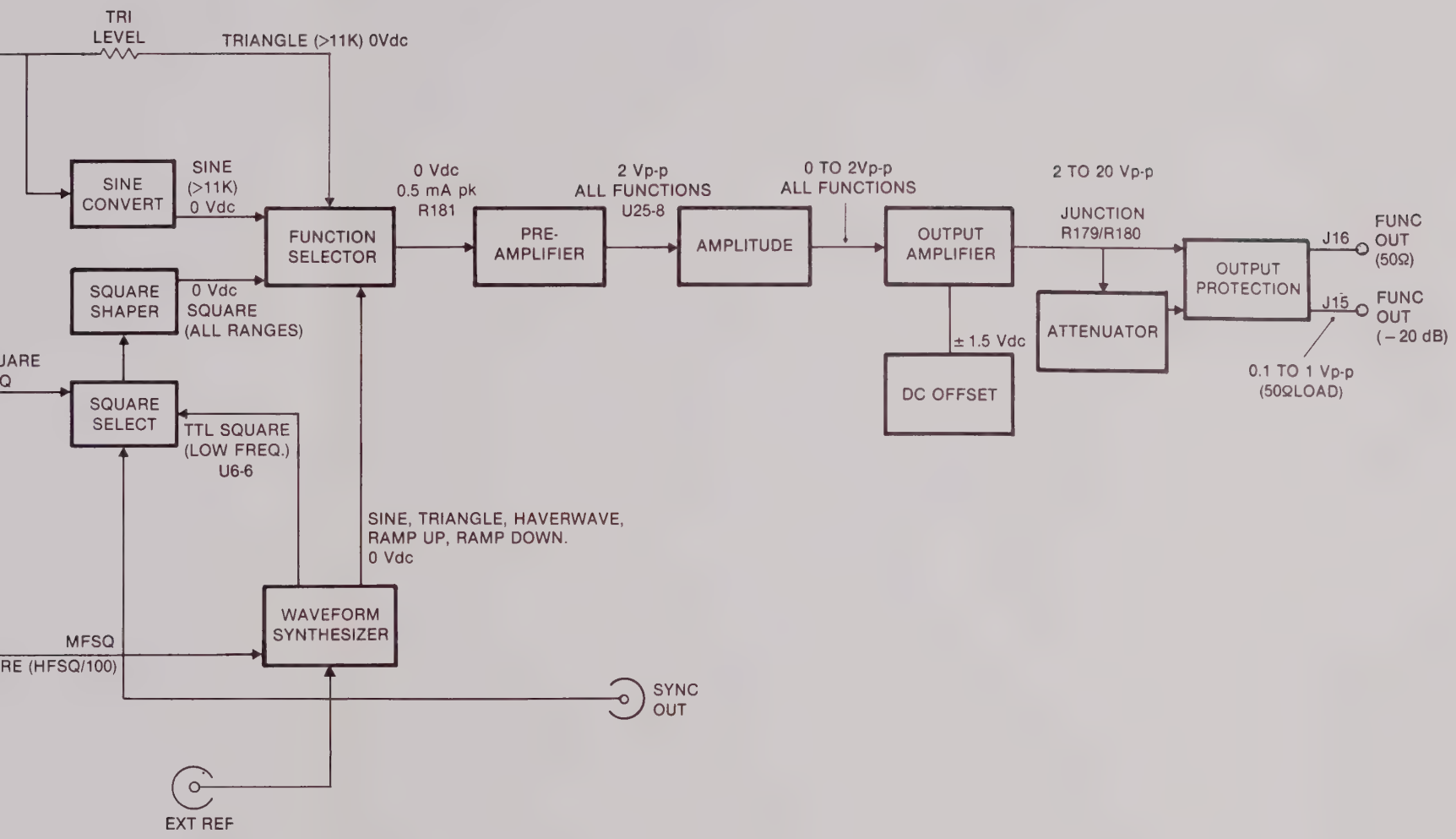


Figure 6-1. Troubleshooting Block Diagram


TRI
LEVEL
TRIANGLE (>11K) 0Vdc
SINE
CONVERT
SINE
(>11K)
0 Vdc
FUNCTION
SELECTOR
0 Vdc
0.5 mA pk
R181
PRE-
AMPLIFIER
2 Vp-p
ALL FUNCTIONS
U25-8
AMPLITUDE
0 TO 2Vp-p
ALL FUNCTIONS
OUTPUT
AMPLIFIER
2 TO 20 Vp-p
JUNCTION
R179/R180
OUTPUT
PROTECTION
J16
FUNC
OUT
(50Ω)
J15
FUNC
OUT
(–20 dB)
ATTENUATOR
± 1.5 Vdc
DC OFFSET
0.1 TO 1 Vp-p
(50ΩLOAD)
SQUARE
SHAPER
0 Vdc
SQUARE
(ALL RANGES)
UARE
Q
SQUARE
SELECT
TTL SQUARE
(LOW FREQ.)
U6-6
SINE, TRIANGLE, HAVERWAVE,
RAMP UP, RAMP DOWN.
0 Vdc
WAVEFORM
SYNTHESIZER
MFSQ
RE (HFSQ/100)
SYNC
OUT
EXT REF

SECTION 6
TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration for repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description (Section 4) in conjunction with the schematics (Section 7). Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

The intent of this section is to provide the information required to return this instrument to proper operation. Information is divided into two parts. Part one contains the overall instrument troubleshooting block diagram (figure 6-1), which is useful in isolating defective blocks within the instrument. Part two consists of a series of circuit guides (paragraph 6.3), one for each block shown in figure 6-1, each guide provides settings and measurements for troubleshooting an individual block. Also, each circuit guide references related schematics, circuit descriptions, and calibration procedures.

Before beginning the troubleshooting process, verify the instrument's controls are set correctly. For example, the instrument cannot produce a 100 kHz ramp up. For more information about instrument operation, refer to section 3 of this manual.

Also, rule out calibration as a possible problem. For instance, if the 10 kHz triangle amplitude is out of specification while the sine and square amplitudes are in specification, then the TRI LEVEL pot, R126, quite possibly, needs adjustment.

Finally, inspect the instrument's components, wiring, and circuit boards for heat damage.

6.2.1 Isolating a Problem

To successfully troubleshoot this instrument, the symptom must first be identified, the faulty block isolated, the block analyzed, and the defective component located and replaced.

To identify the symptom, use all the front panel controls and connectors. Pay particular attention to the frequency range, as this identifies the signal flow (function generator loop or synthesizer).

Once the signal flow is established, figure 6-1 can be used to isolate the circuit block. Start measuring the outputs of the circuit block until the defective block is located.

Once the block is isolated, refer to the appropriate circuit guide; see table 6-1. Set the controls as instructed and take the measurements given to check out the block. Paragraph 6.4 gives component troubleshooting information.

6.3 TROUBLESHOOTING GUIDES

Table 6-1. Circuit Guides

Circuit Guide	Paragraph
VCG	6.3.1
Current Source and Sink	6.3.2
Current Sink and Trigger Control	6.3.3
Current Switch	6.3.4
Frequency Range	6.3.5
Triangle Buffer	6.3.6
Comparator, Switch and Square Buffers	6.3.7
High Frequency Compensation	6.3.8
Trigger Logic	6.3.9
Waveform Synthesizer	6.3.10
Stabilizer	6.3.11

Table 6-1. Circuit Guides (Continued)

Circuit Guide	Paragraph
Square Selector	6.3.12
Square Shaper	6.3.13
Sine Converter	6.3.14
Function Selector	6.3.15
Preamplifier	6.3.16
Output Amplifier	6.3.17
Attenuator	6.3.18
Output Protection	6.3.19
Pushbutton Interface	6.3.20
Power-On Reset	6.3.21
Mode Control	6.3.22
Misc Control	6.3.23
Frequency Range Control	6.3.24
Function Control	6.3.25
Display	6.3.26
Power Supply	6.3.27

6.3.1 VCG

Related information in this manual
Schematic: 0103-00-1116 sheet 1.
Circuit Description: Paragraph 4.2.1.1.
Calibration Procedure: Table 5-1, Steps 11, 12, and 17.

Set the frequency controls as indicated in table 6-2, and take the measurements; the stabilizer must be off.

Table 6-2. VCG

Frequency Knobs	P5-B4	J7-2	U1-1
Both full cw	+15V	0V	−7.5V
Both full ccw	+1.36V	−15V	∼0V

Related digital control lines.
VCG KILL: TTL low = VCG In connected;
TTL high = VCG disconnected.

6.3.2 Current Source and Sink

Related information in this manual.
Schematic: 0103-00-1116 Sheet 1.
Circuit Description: Paragraph 4.2.1.1.
Calibration Procedure: Table 5-1, Steps 13, 14, and 15.

Set the controls as shown and make the checks in tables 6-3 and 6-4.

Control	Settings
VCG In	0V
Stab	Off
Frequency knobs	As directed
Freq Range	1.100 kHz

Table 6-3. Current Source

Frequency Knobs	U1-1	U1-9	U1-8	Base Q2
Both full cw	−7.5V	0V	∼1.3V	∼+11.8V
Both full ccw	∼0V	0V	∼0.5V	∼+14.5V

Table 6-4. Current Sink

Frequency Knobs	R42-16	R42-14	R42-3	U28-1
Both full cw	+2.5V	−2.5V	0V	−11.8V
Both full ccw	+2.26 mV	−2.26 mV	0V	∼−14.5V

6.3.3 Current Sink and Trigger Control

Related information in this manual.
Schematic: 0103-00-1116 Sheet 1.
Circuit Description: Paragraph 4.2.1.1.

Set the controls as shown, and perform the checks in tables 6-5 and 6-6.

Control	Settings
Frequency knobs	As directed
Freq Range	1.100 kHz
VCG In	0V

Table 6-5. Current Sink and Trigger Control

Frequency Knobs	U28-1	U28-7
Both full cw	−11.8V	−12.5V
Both full ccw	∼−14.5V	∼−15V

Control	Settings
Frequency knobs	Both cw
Freq Range	1.100 kHz
VCG In	0V
Mode	As directed

Table 6-6. Trigger Control

Mode	RUN	Anode CR7	Cathode CR7
Cont	High	+2.1V	−0.7V
Trig	Low	−1.1V	−0.7V

6.3.4 Current Switch

Related information in this manual.
Schematic: 0103-00-1116 Sheet 2.
Circuit Description: Paragraph 4.2.1.2.

Set the controls as shown; and take the measurements as shown in figure 6-2.

Control	Settings
Frequency knobs	Both cw
Freq Range	1.100 kHz
Stab	Off
Mode	Cont

6.3.5 Frequency Range Switches

Related information in this manual.
Schematic: 0103-00-1116 Sheet 2.
Circuit Description: Paragraph 4.2.1.3.
Calibration Procedure: Table 5-1, Steps 20, 21, and 22.

The table 6-7 lists the logic levels for the nine frequency ranges; a low enables the range capacitor, and a high disables the range capacitor. Table 6-8 gives measurement values for a single typical range switch ($\overline{FR6}$); these levels are typical of all three switches.

Table 6-7. Frequency Range (TTL levels)

Range	$\overline{FR6}$	$\overline{FR5}$	$\overline{FR4}$
11.00 MHz	High	High	High
1.100 MHz	Low	High	High
110.0 kHz	High	Low	High
11.00 kHz	High	High	Low
1.100 kHz	Low	High	High
110.0 Hz	High	Low	High
11.00 Hz	Low	High	High
1.100 Hz	High	Low	High
110.0 mHz	High	High	Low

Table 6-8. Frequency Range ($\overline{FR6}$ shown, typical)

$\overline{FR6}$	Low	High
Base Q22	+3.6 Vdc	+4.0 Vdc
Emitter Q22	+4.3 Vdc	+4.3 Vdc
Collector Q22	+4.0 Vdc	−15 Vdc
Junction R108 and R109	+1.4 Vdc	−15 Vdc
Junction R106 and R107	−7.5 Vdc	−7.5 Vdc

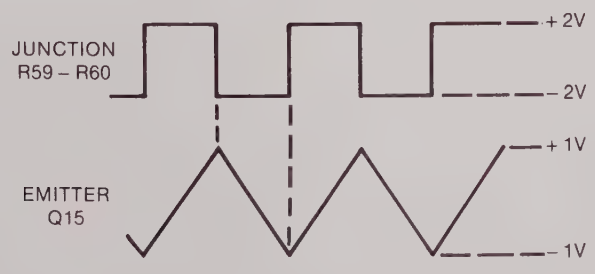


Figure 6-2. Current Switch Waveforms

6.3.6 Triangle Buffer

Related information in this manual.
Schematic: 0103-00-1116 Sheet 2.
Circuit Description: Paragraph 4.2.1.4.
Calibration Procedure: Table 5-1; Steps 5 and 10.

Set the controls as shown, and take the measurements as shown in figure 6-3 and table 6-9.

Control	Settings
Power	Turn Off; then On
Frequency knobs	Both cw
Mode	As directed

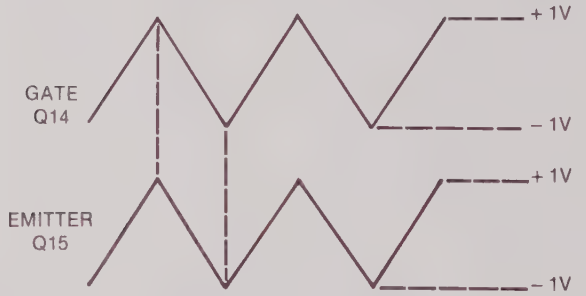


Figure 6-3. Triangle Buffer (Cont Mode)

Table 6-9. Triangle Buffer (Trigger Mode)

Test Point	Desired Results
Q14 Gate	0Vdc
Q14 Source	+0.7V
Q21 Base	–5V
Q15 Emitter	0Vdc

6.3.7 Comparator, Switch and Square Buffers

Related information in this manual.
Schematic: 0103-00-1116 Sheet 2.
Circuit Description: Paragraphs 4.2.1.5, 4.2.1.6, and 4.2.4.1.

Set the controls as shown; then take the measurements as shown in figure 6-4.

Control	Settings
Power	Turn Off; then On
Frequency knobs	Both full cw

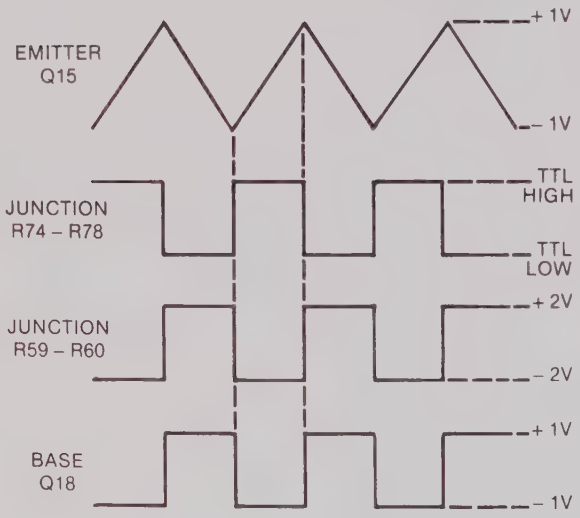


Figure 6-4. Comparator, Switch and Square Buffer

6.3.8 High Frequency Compensation

Related information in this manual.
Schematic: 0103-00-1116 Sheet 2.
Circuit Description: Paragraph 4.2.1.7.
Calibration Procedure: Table 5-1, Steps 6 and 23.

Set the controls as shown, and then take the measurements as shown in tables 6-10 and 11.

Control	Settings
Power	Turn Off; then On
Frequency knobs	Both cw

Table 6-10. Low Frequency Check (<1.1 MHz Range)

Test Point	Desired Results
U27-3	0Vdc
U27-2	0Vdc
U27-6	+0.7Vdc
Q5 Collector	+10 Vdc
Q16 Base	–10 Vdc
Q6 Emitter	+10.7 Vdc
Q16 Emitter	–10.7 Vdc

Table 6-11. High Frequency Compensation (11 MHz Range)

Select the 11 MHz range.

Test Point	Desired Results
U27-3	−5Vdc
U27-6	−4.3 Vdc
Q5 Collector	+11.7 Vdc
Q16 Base	−11.7 Vdc
Q6 Emitter	+12.4 Vdc
Q16 Emitter	−11.4 Vdc

Related digital control logic.

$\overline{FR7}$ goes low on the 11 MHz range;
$\overline{FR7}$ remains high on all other ranges.

6.3.9 Trigger Logic

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.1.8.

Table 6-12 lists the control lines related ot the trigger logic circuit.

Table 6-12. Trigger Logic

Control Line	Description
Trig In	External trigger input signal.
Man Trig	Front panel manual trigger. Goes low when pushbutton is pressed.
MC0	A control line from the mode control logic. Triggered Sweep, Trigger, and Gate modes: TTL high. Continuous: TTL low.
MC1	A control line from the mode control logic. Gate and Continuous modes: TTL low.
$\overline{KILL}$	A control line from the function control logic. This line goes low when the dc function is selected. The line remains high for all other functions.
HFSQ	TTL level square wave from the function generator loop.
LF	A control line from the frequency range control logic. 11 MHz, 1.1 MHZ, 110 kHz, 11 kHz ranges: TTL low.

Table 6-12. Trigger Logic (Continued)

Control Line	Description
RUN	A control line that enables or disables the function generator loop. A TTL low turns the generator off, and a TTL high turns the generator on.

6.3.10 Waveform Synthesizer

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.2.

Review the circuit description (paragraph 4.2.2) before using troubleshooting the waveform synthesizer; then use the following hints. Remember, the waveform synthesizer produces waveforms on the 1.100 kHz and below ranges.

1. Check the counter's clock input: U15-11, U14-2, U10-2. With $\overline{EPC}$ high, the internal reference is selected, and external reference is selected when $\overline{EFC}$ is low.
2. Verify the up/down counter's data lines change with each clock pulse: U6-3, U14-14, U14-13, U14-12, U14-11, U10-14, U10-13, U10-12, U10-11.
3. Verify the up/down control lines switch coincident with the positive and negative peaks: U17-11, U17-8, U10-1, U14-1.
4. Verify data lines from EPROM (U9) change. Also verify correct waveform selection using FS0 and FS1.

Function	FS0	FS1
DC	0	0
Sine	0	0
Triangle	0	1
Ramp Up	1	0
Ramp Down	1	1

5. Verify the data lines from the latch (U8) change.
6. Check U7 pin 4 for the correct waveform.
7. Check $\overline{SYNTH}$ (U5-16) for a low.

6.3.11 Stabilizer

Related information in this manual.
Schematic: 0103-00-1115 Sheets 2 and 3.
Circuit Description: Paragraph 4.2.3.

The circuit description's text, tables, and figures contains the necessary information to troubleshoot the stabilizer circuit.

6.3.12 Square Selector

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.4.2.

Set the controls as shown; then take the measurement as shown in table 6-13.

Control	Settings
Freq Range	As specified
Frequency knobs	Both full cw
Mode	Cont

Table 6-13. Square Selector

Frequency Range	LF Control Line	Square Source	TTL SQ (Output)
⩾11.00 kHz	Low	HFSQ (Function Generator Loop)	Square wave in phase HFSQ
<11.00 kHz	High	U6-6 (LFSQ) (Waveform Synthesizer)	Square wave in phase with LFSQ

6.3.13 Square Shaper

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.4.3.
Calibration Procedure: Table 5-1, Steps 27, 28, and 29.

Set the controls as shown, and take the measurements shown in figure 6-5.

Control	Settings
Power	Turn Off; then On
Frequency knobs	Both full cw
Function	Square
Mode	Cont

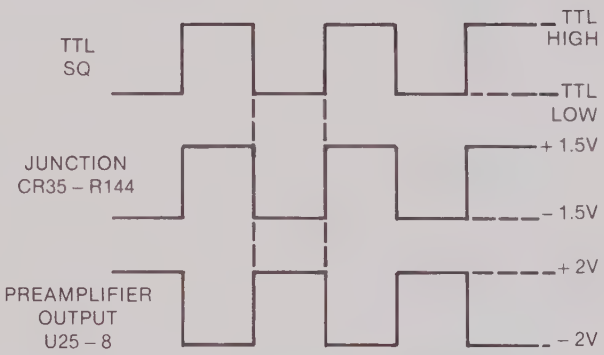


Figure 6-5. Square Shaper

6.3.14 Sine Converter

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.4.4.
Calibration Procedure: Table 5-1, Step 16.

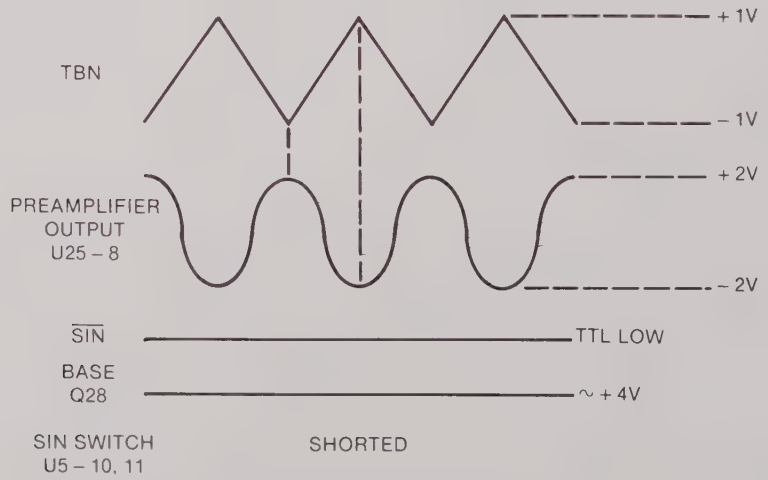


Figure 6-6. Sine Converter

Set the controls as shown, and take the waveform measurements as shown in figure 6-6.

Control	Settings
Frequency knobs	Both full cw
Freq Range	⩾11.00 kHz
Mode	Cont
Function	Sine

NOTE

Time symmetry and dc offset of triangle affects the sine distortion; refer to the calibration procedure, steps 12 to 15.

On the 1.100 kHz range and below, the waveform synthesizer creates the sine wave. Thus, the sine converter has no affect on the lower five frequency ranges.

6.3.15 Function Selector

Related information in this manual.
Schematic: 0103-00-1116 Sheet 3.
Circuit Description: Paragraph 4.2.4.5.

The function selector, which consists of four switches, routes the various functions to the preamplifier. Only one switch will be closed at a time.

Table 6-14 describes the function selector control lines. A logic low which originates at the function control logic circuit, closes the respective switch.

Table 6-14. Function Selector

Control Line	Description
$\overline{\text{SYNTH}}$	At frequencies below the 11.00 kHz range, selects signals from waveform synthesizer.
$\overline{\text{SQR}}$	At frequencies on or above 11.00 kHz range, selects square wave.
$\overline{\text{TRI}}$	At frequencies above on or 11.00 kHz range, selects triangle wave.
$\overline{\text{SIN}}$	At frequencies on or above 11.00 kHz range, selects sine wave.

6.3.16 Preamplifier

Related information in this manual.
Schematic: 0103-00-1116 Sheet 4.
Circuit Description: Paragraph 4.2.4.6.
Calibration Procedure: Table 5-1, Step 24.

DC Problems

Set the controls as shown; then perform the checks in table 6-15.

Control	Settings
Function	DC
DC Offset	Off

Table 6-15. Preamplifier

Test Point	Desired Results
U25 pin 14	0 ± .02Vdc
E1	0 ± .05Vdc

Function Problems

Set the controls as shown, and measure the waveform at E1: ±2V sine wave.

Control	Settings
Power	Turn Off; then On
D.C. Offset	Off
Amplitude	Full cw

6.3.17 Output Amplifier

Related information in this manual.
Schematic: 0103-00-1116 Sheet 4.
Circuit Description: Paragraph 4.2.4.7.
Calibration Procedure: Table 5-1, Step 9.

Set the controls as shown; then take the waveform measurements. Refer to table 6-16.

Control	Settings
Function	DC
D.C. Offset	Off

Table 6-16. Output Amplifier

Test Point	Desired Results
Junction R179 and R180	~0Vdc
Junction R166 and R190	~0Vdc
P5 pin B8	0Vdc
Junction R172 and R169	+14 Vdc
Junction R192 and R169	−14 Vdc
Across R165	14.3 Vdc
Across R171	1.5 Vdc
U26 pin 10	+12.8 Vdc
U26 pin 13	+12.8 Vdc
U26 pin 7	+5.7 Vdc

6.3.18 Attenuator

Related information in this manual.
Schematic: 0103-00-1116 Sheet 4.
Circuit Description: Paragraph 4.2.4.8.
Calibration Procedure: Table 5-1, Step 37.

Set the controls as shown; then take the waveform measurements. Refer to figure 6-7.

Control	Settings
Power	Turn Off; then On
D.C. Offset	Off
Amplitude	Full cw

NOTE

Terminate the Function Out (– 20 dB) with 50Ω load.

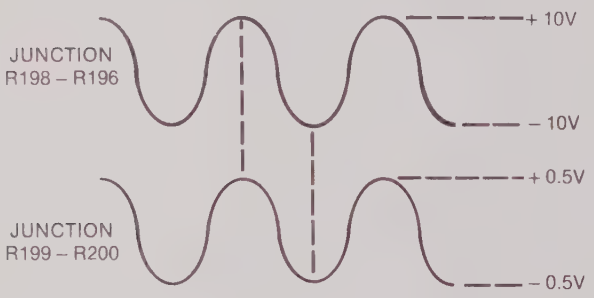


Figure 6-7. Attenuator

6.3.19 Output Protection

Related information in this manual.
Schematic: 0103-00-1116 Sheet 4.
Circuit Description: Paragraph 4.2.4.9.

Set the controls as shown; make the following checks.

Control	Settings
Power	Turn Off; then On
Amplitude	Full cw
D.C. Offset	Off

Note

Power must be turned off before checking fuses and diodes.

Check fuses (F1, F2) if there is no output at the Function Out (50Ω) BNC. Check for shorted diodes (CR50, CR51, CR2, CR3) if the fuses are ok. Check fuses (F3, F4) if there is no output at the Function Out (– 20 dB) BNC.

6.3.20 Pushbutton Interface

Related information in this manual.
Schematic: 0103-00-1115 Sheet 1.
Circuit Description: Paragraph 4.2.5.

Check the pushbutton interface circuit by pressing the appropriate front panel pushbutton and making the checks: refer to table 6-17.

Table 6-17. Pushbutton Interface

Pushbutton	Logic Level	Interface	Logic Level	Control Line
Trigger	high	U3G-8	low	MAN TRIG
Stab	low	U3G-2	high	STABPB
Function ←	low	U2G-8	high	FUNCDN
Function →	low	U2G-6	high	FUNCUP
Mode ←	low	U2G-10	high	MODDN
Mode →	low	U2G-12	high	MODUP
Freq Range ←	low	U2G-2	high	FRDN
Freq Range →	low	U2G-4	high	FRUP
Ref	high	U3G-10	low	EFCPB
Haver	low	U3G-6	high	HAVER

6.3.21 Power-On Reset

Related information in this manual.
Schematic: 0103-00-1115 Sheet 3.
Circuit Description: Paragraph 4.2.6.1.

Turn the power off, wait about one minute, and then turn the power on. Take the waveform measurements as shown in figure 6-8.

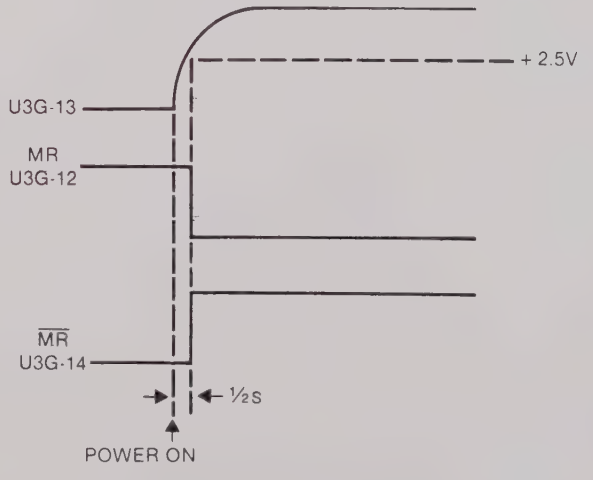


Figure 6-8. Power-On Reset

Table 6-18. Mode Control

Mode	U4G				MC0	MC1	SWPT	$\overline{SWP}$	SWP	$\overline{GATE}$	$\overline{TRIG}$	$\overline{CONT}$	BL (2)
	QD	QC	QB	QA									
Gate	0	1	0	1	1	1	0	1	0	0	1	1	1
Trig	0	1	1	0	1	0	0	1	0	1	0	1	1
Cont (1)	0	1	1	1	0	1	0	1	0	1	1	0	0

Notes
1 Power-On Reset mode
2 Assumes $\overline{EFC} = 1$

6.3.22 Mode Control

Related information in this manual.
Schematic: 0103-00-1115 Sheet 2.
Circuit Description: Paragraph 4.2.6.2.

Set the instrument to the desired mode. Compare the logic levels as shown in table 6-18.

6.3.23 Misc Control

Related information in this manual.
Schematic: 0103-00-1115 Sheet 2.
Circuit Description: Paragraph 4.2.6.3.

The circuit description's text contains the necessary information to troubleshoot the misc circuit.

6.3.24 Frequency Range Control

Related information in this manual.
Schematic: 0103-00-1115 Sheet 2.
Circuit Description: Paragraph 4.2.6.4.

Set the instrument to the desired frequency range and check the logic level as shown in table 6-19.

Table 6-19. Frequency Range Control

Max (Hz)	U6E				$\overline{LF}$	$\overline{\div 100}$	FR4	FR5	FR6	$\overline{FR7}$	DDP1	DDP2	$\overline{DDP3}$	DMHz	DK	DHz	$\overline{DmHz}$	Actual Gen Freq
	QD	QC	QB	QA (1)														
11.00M	1	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0	1	11 M
1.100M	1	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	1	1.1 M
110.0k	0	1	1	1	0	1	0	1	0	1	0	0	0	0	1	1	1	110 k
11.00k	0	1	1	0	0	1	1	0	0	1	0	1	1	0	1	1	1	11k
1.100k(2)	0	1	0	1	1	1	0	0	1	1	1	0	1	0	1	1	1	1.1M
110.0k	0	1	0	0	1	1	0	1	0	1	0	0	0	0	0	1	1	110k
11.00	0	0	1	1	1	0	0	0	1	1	0	1	1	0	0	1	1	1.1M
1.100	0	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	1	110k
110.0m	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	11k

Notes
1 Assumes Internal Reference.
2 Power-On Reset mode.

Table 6-20. Function Control

Function	QD	QC	QB	QA	FS0	FS1	$\overline{SIN}$	$\overline{TRI}$	$\overline{SYNTH}$	$\overline{\sim}$	$\overline{\sqcap}$	$\overline{\sim}$	$\overline{KILL}$	$\overline{\diagdown}$	$\overline{\diagup}$
DC	0	0	1	1	0	0	1	1	1	1	1	1	0	1	1
Sine	0	0	1	0	0	0	0	1	0	1	1	0	1	1	1
Square	0	0	0	1	0	0	1	1	1	1	0	1	1	1	1
Triangle	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1
Ramp Up	1	1	1	1	1	0	1	1	0	1	1	1	1	1	0
Ramp Dn	1	1	1	0	1	1	1	1	0	1	1	1	1	0	1

Notes
1 For this table LF = 0.
2 LF = 1 for Ramp Up and Ramp Down.
3 If LF = 1 (high) then $\overline{SIN}$ and $\overline{TRI}$ always high and $\overline{SYNTH}$ always low.
4 Power-On Reset condition, except $\overline{SIN}$ high and $\overline{SYNTH}$ low.

6.3.25 Function Control

Related information in this manual.
Schematic: 0103-00-1115 Sheet 2.
Circuit Description: Paragraph 4.2.6.5.

Set the controls as shown, and check the logic levels as shown in table 6-20.

Control	Settings
Freq Range	11.00 kHz
Function	As needed

6.3.26 Display

Related information in this manual.
Schematic: 0103-00-1117.
Circuit Description: Paragraph 4.2.7.

Figure 6-9 illustrates a typical display segment while table 6-21 identifies the annunciators and thier control lines. 5Vrms must appear between the control line and BL.

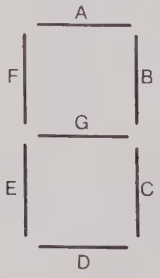


Figure 6-9. Typical Digit Segment Assignments

Table 6-21. Display Control Lines

Display	Control Line
1st Digit	1 B/C
2nd Digit	2A, 2B, 2C, 2D, 2E, 2F, 2G
3rd Digit	3A, 3B, 3C, 3D, 3E, 3F, 3G
4th Digit	4A, 4B, 4C, 4D, 4E, 4F, 4G
k	K
Hz	Hz
MHz	MHz
mHz	mHz
Stab On	X1
Stab Off	X2
Gate Mode	Z1
Trig Mode	Z2
Cont Mode	Z3
DC Function	Z7
Sine Function	Z8
Square Function	Z9
Triangle Func	Z10
Ramp Up	Z11
Ramp Down	Z12
1st Dec Pt	DP1
2nd Dec Pt	DP2
3rd Dec Pt	DP3
Hav On	X5
Hav Off	X6
Int Ref	X7
Ext Ref	X8

Table 6-22. Power Supply

Supply	Voltage Tolerance	Test Point	Maximum Input Ripple	Test Point	Maximum Output Ripple	Test Point
+15V	±350 mV	C7	3Vac	C2	0.02Vac	C7
−15V	±350 mV	C8	3Vac	C3	0.02Vac	C8
+5V	±250 mV	C12	3Vac	C10	0.02Vac	C12

6.3.27 Power Supply

Related information in this manual.
Schematic: 0103-00-1113.
Circuit Description: Paragraph 4.2.8.
Calibration Procedure: Table 5-1, Steps 1 through 4.

1. For fuse replacement, refer to paragraph 2.2.3.
2. To determine a faulty power supply; check for the voltages given in table 6-22.
3. If the pass devices' input tests bad, remove power and connector J3. Check for:
   (a) Blown fuse.
   (b) Shorted or open diodes (CR1, CR2).
   (c) Shorted or open capacitors (C2, C3, C4, C5, C10, C11) at the input the pass devices.
   (d) Short between the pass devices' metal mounting tab and chassis ground.
   (e) Bad transformer.
4. If the regulators input is good, remove power and connectors J4 and J5. Check for:
   (a) Shorted capacitors at the regulator's output.
   (b) Short between pass devices' mounting tab and chassis ground.
   (c) Excessive loading by board circuits; to verify, disconnect by removing either J4 or J5.
   (d) Check +15V and −15V pass devices for normal transistor operation.
   (e) If all of the above conditions appear normal, replace the voltage regulator; VR1 for +5V and VR2 for +15V and −15V.

6.4 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.4.1 Transistor

1. A transistor is defective if more than 1V is measured across its base-emitter junction in the forward direction.
2. A transistor, when used as a switch, may have a few volts reverse bias voltage across the base-emitter junction.
3. If the collector an emitter voltages are the same, but the base emitter voltage is less than 500 mV forward voltage or reversed bias, the transistor is defective.
4. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base-emitter junction should be off (no collector current); otherwise one of the transistors is defective.

6.4.2 Diode

A diode (except a zener) is defective if there is greater than 1Vdc (typically 0.7Vdc) forward voltage across it.

6.4.3 Operational Amplifier

1. Generally the "+" and "−" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.
2. When the output of the amplifier is connected to the "−" input (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operation amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.4.4 FET Transistor

1. No measurable gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective. Gate-to-source voltage is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for 2N5485 and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.

6.4.5 Capacitor

1. Shorted capacitors have 0V across their terminals.
2. Open capacitors can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.
3. Leaky capacitors will often have a decreased voltage across their terminals.

SECTION 7
PARTS LIST AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below. Special-order and option drawings, if any, will follow these standard drawings.

7.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, and unit serial number.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

DRAWING	DRAWING NUMBER
Model 21 Assembly Drawing	1000-00-1111
Instrument Outline Drawing	0002-00-1111
Instrument Schematic	0004-00-1111
Stabilizer Control Board Assembly	1100-00-1115
Stabilizer Control Board Schematic	0103-00-1115
Stabilizer Control Board Parts List	1100-00-1115
Waveform Generator Board Assembly	1100-00-1116
Waveform Generator Board Schematic	0103-00-1116
Waveform Generator Board Parts List	1100-00-1116
Front Panel Assembly	1101-00-1112
Display Assembly	1208-00-1117
Display Schematic	0103-00-1117
Power Supply Assembly	1101-00-1113
Power Supply Schematic	0103-00-1113
Power Supply Board Assembly	1208-00-1118
AC Primary Board Assembly	1208-00-1119

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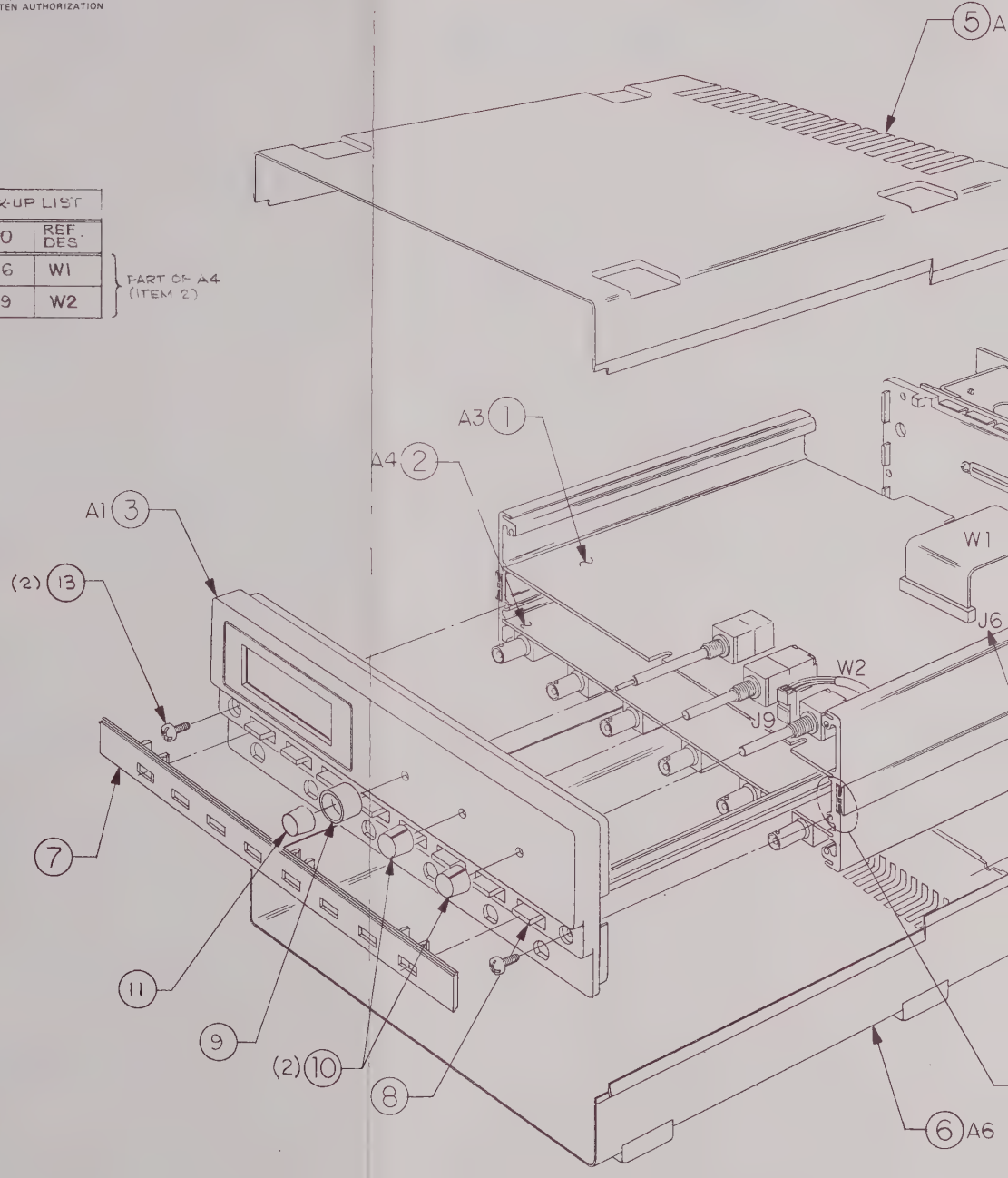
CABLE HOOK-UP LIST			
FROM	TO	REF DES	
P6	J6	W1	PART OF A4 (ITEM 2)
P9	J9	W2	

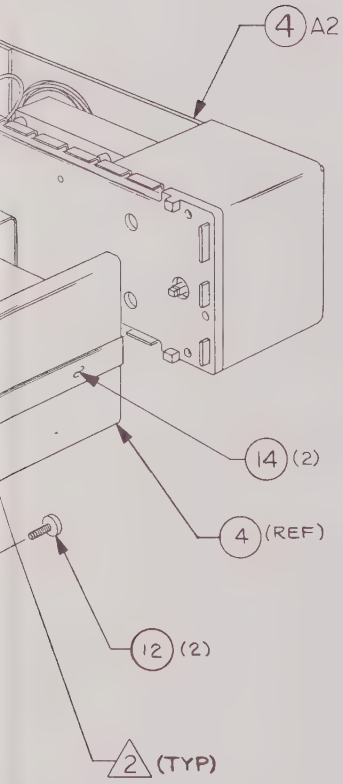


2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
1. SEE 0004-00-1111 FOR INSTRUMENT SCHEMATIC.

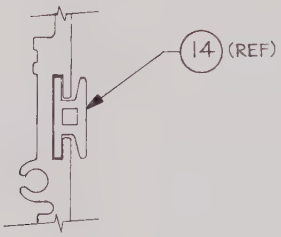
NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-3894

REV	ECN	BY	DATE	APP
F	4881	MF		



E DETAIL "A"



DETAIL "A"
(SCALE:2/1)

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	OUTLINE DRWG, INST	0002-00-1111	WVTK	0002-00-1111	1
NONE	SCHEMATIC, INST	0004-00-1111	WVTK	0004-00-1111	1
NONE	CALIB PROCEDURE	0006-00-1111	WVTK	0006-00-1111	1
NONE	ENG SPECIFICATIONS	0007-00-1111	WVTK	0007-00-1111	1
1	PCA, STAB. /CONTROL	21-1115	WVTK	1100-00-1115	1
2	PCA, WAVEFORM GEN	21-1116	WVTK	1100-00-1116	1
3	ASSY, FRONT PANEL (MODEL 21)	21-1112	WVTK	1101-00-1112	1
4	ASSY, POWER SUPPLY	21-1113	WVTK	1101-00-1113	1
5	ASSY, TOP COVER	21-1114	WVTK	1201-00-1114	1
NONE	ASSY, BOTTOM COVER	1206-00-1301	WVTK	1206-00-1301	1
NONE	ASSY, CABLE KIT	21-1120	WVTK	1207-00-1120	1
NONE	INSTRUCTION MANUAL	MANUAL-21	WVTK	1300-00-1111	1
7	BEZEL, KEY(MODEL 21)	21-6160	WVTK	1400-01-6160	1
8	POWER ROD	21-6201	WVTK	1400-01-6201	1
14	INSERT, SIDE PANEL	20-7910	WVTK	1400-01-7910	2
10	KNOB, GRAY, SMALL W/LINE, 1/4 BUSHING	2400-01-0031	WVTK	2400-01-0031	2
11	KNOB, GRAY, SMALL 1/8 BUSHING	2400-01-0032	WVTK	2400-01-0032	1
9	KNOB, GRAY, CONCENTRIC OUTER	2400-01-0034	WVTK	2400-01-0034	1
12	SCREW, TRUSS HD, CROSS RECESS, 10-32X3/8	10-32 X 3/8	CMRCL	2800-20-0106	2
13	SCREW, S/T TYPE B, P.H. CROSS RECESS, 8X1/2	8-18 X 5/8	CMRCL	2800-22-8910	2
NONE	INSERT	101-18	WVTK	3300-00-0019	1
NONE	CARTON	101-18A	WVTK	3300-01-0012	1
NONE	PWR CORD	6001-80-0005	WVTK	6001-80-0005	1

REMOVE ALL BURRS AND BREAK SHARP EDGES
DRAWN TALMADGE 7-11-83
MATERIAL
PROJ ENGR
RELEASE APPROV
FINISH WAVETEK PROCESS
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030
DO NOT SCALE DWG
SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
MODEL 21, 11 MHz STAB. FUNCTION GENERATOR

MODEL NO 21
DWG NO 1000-00-1111
REV F
CODE IDENT 23338
SHEET 1 OF 1

1000-00-1111 F

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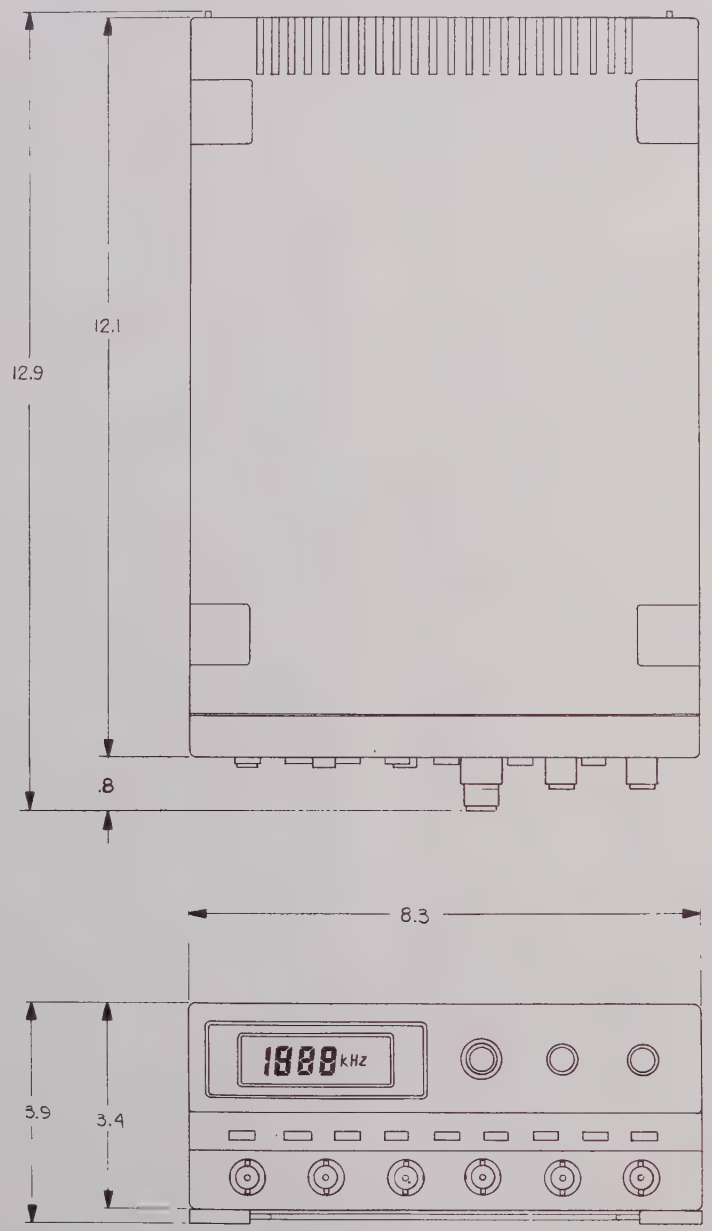
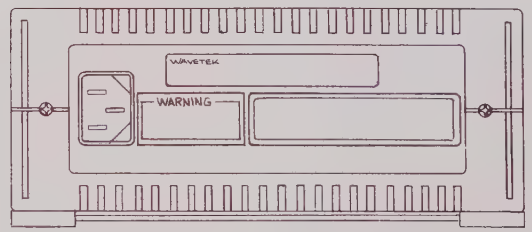
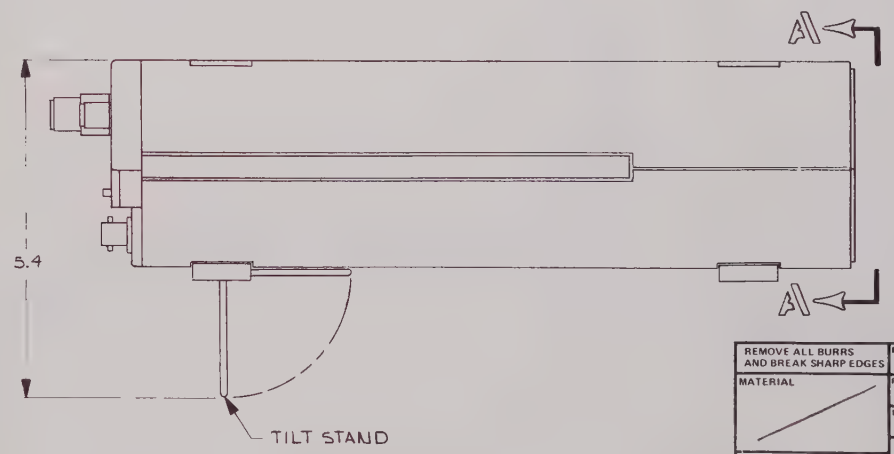
REV	ECN	BY	DATE	APP





VIEW A1-A1



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. Magnolia	DATE 6-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE OUTLINE DRAWING INSTRUMENT
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO 21/22
	DO NOT SCALE DWG		DWG NO 0002-00-1111 REV
	SCALE 3/4 = 1		CODE IDENT 23338 SHEET 1 OF 1

0002-00-1111

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REV	ECN	BY	DATE	APP

A2
ASSY, POWER SUPPLY
1101-00-1113

A2A2
PCA, AC PRIMARY
1208-00-1119

AC POWER
J1
E1
W4
GRN/YEL
E2
F1
3/8 A SB, 115V
3/16 A SB, 230V
115V
230V
J2
P2
P2 ORIENTATION FOR 230V AC INPUT
FROM T1
GRY
WHT/BLK
WHT/GRY
BLK

A2T1
5600-00-0027

RED
RED
WHT/RED
BLU
BLU
P3
J3
W3
GRN/YEL
E3

A2A1
PCA, POWER SUPPLY
1208-00-1118

J4 P4

HFSQ	A 1
MFSQ	A 2
FR4	A 3
FR5	A 4
-15V	A 5
+5V	A 6
+5V	A 7
+15V	A 8
LIN	A 9
FR7	A 10
DIG GND	B 1
DIG GND	B 2
FR6	B 3
FRCOARSE	B 4
ANALOG GND	B 5
ANALOG GND	B 6
ASWP	B 7
AOFST	B 8
DIG GND	B 9
DIG GND	B 10

J5 P5

HFSQ	A 1
MFSQ	A 2
FR4	A 3
FR5	A 4
-15V	A 5
+5V	A 6
ASWP	A 7
+15V	A 8
LIN	A 9
FR7	A 10
GND	B 1
GND	B 2
FR6	B 3
FRCOARSE	B 4
GND	B 5
GND	B 6
GND	B 7
AOFST	B 8
GND	B 9
GND	B 10

J6 P6
DIG GND, FR FINE, TRIG, KILL, VCG, LOG, STR, TRI, MAN TRIG, SQR, MCI, MCO, SYNTH, SWP RUN, FSO, EFC, THAV, LF, 50 KHZ, FS1
J9 P9
PRE AMP OUT, PRE AMP GND, PWR AMP IN
W1
W2
J7
J10
TEST CONNECTOR
VCGTST, GND, TRITST, GND, -15V, +5V, +15V, RUNTST, FUNCTST, COMPTST, GND, N.C, GND, GCVTST
E2 E1 E3 E4

A4
PCA, WAVEFORM GEN
1100-00-1116 (MODEL 21)
1100-00-1121 (MODEL 22)

J11 VCG IN
J12 TRIG IN
J13 REF IN (MODEL 21) SWEEP OUT (MODEL 22)
J14 SYNC OUT
J15 FUNC OUT (-20dB)
J16 FUNC OUT (50Ω)

A3
PCA, STAB,/CONTROL
1100-00-1115 (MODEL 21)
1100-00-1123 (MODEL 22)

A1
ASSY, FRONT PANEL
1101-00-1112 (MODEL 21)
1101-00-1122 (MODEL 22)

A1A1
PCA, DISPLAY
1208-00-1117

P8 J8

A 1	+5V
A 2	+5V
A 3	GND
A 4	PB6
A 5	PB3A
A 6	PB3B
A 7	PB4A
A 8	PB4B
A 9	GND
A 10	PB1
A 11	BP
A 12	X3
A 13	X4
A 14	Z7
A 15	DP1
A 16	DP3
A 17	4E
A 18	4D
A 19	Z10
A 20	4C
A 21	K
A 22	HZ
A 23	Z11
A 24	Z12
A 25	2F
A 26	1B/C
A 27	X1
A 28	2E
A 29	SPARE
A 30	SPARE
A 31	X8
A 32	3C
A 33	3D
A 34	DP2
A 35	3E
B 1	+5V
B 2	+5V
B 3	PB7
B 4	PB5
B 5	PB2B
B 6	PB2A
B 7	MHZ
B 8	Z6
B 9	X5
B 10	X6
B 11	MHZ
B 12	Z5
B 13	4B
B 14	Z4
B 15	4A
B 16	4F
B 17	4G
B 18	3B
B 19	Z3
B 20	3A
B 21	3F
B 22	3G
B 23	2B
B 24	Z2
B 25	2A
B 26	2G
B 27	Z1
B 28	X2
B 29	SPARE
B 30	SPARE
B 31	X7
B 32	Z9
B 33	2C
B 34	Z8
B 35	2D

1000-00-1111 (MODEL 21)
1000-00-1121 (MODEL 22)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT	DATE 5-18-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR	10-14-83	TITLE SCHEMATIC, INSTRUMENT
FINISH WAVETEK PROCESS	RELEASE APPROV 11/9/83	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	SCALE	MODEL NO 21/22 DWG NO 0004-00-1111 REV
			CODE IDENT 23338 SHEET 1 OF 1

0004-00-1111

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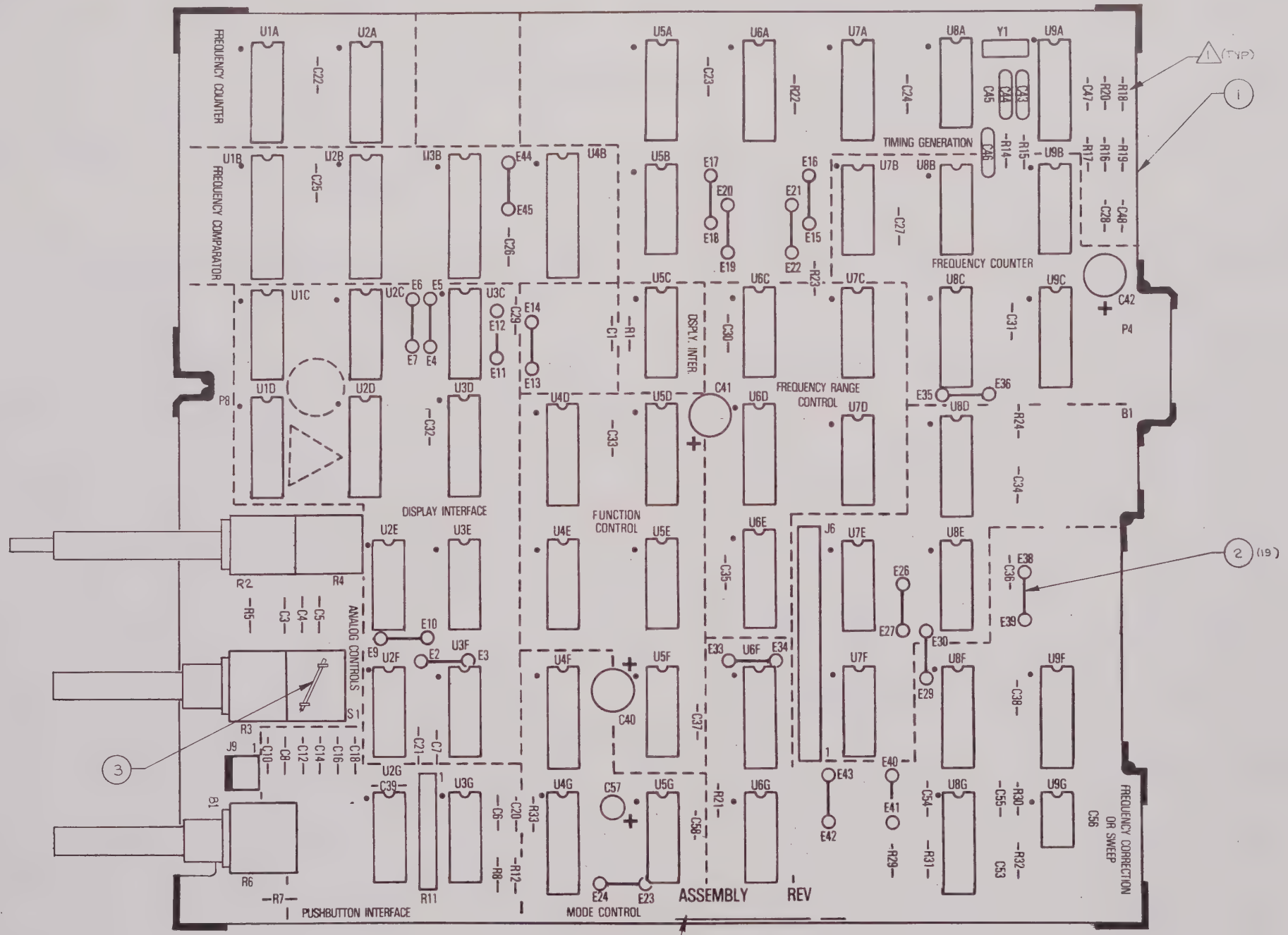

NOTE. UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 6/13/83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR	10-14-83	TITLE PCA, STAB./ CONTROL (A3)
FINISH WAVETEK PROCESS —	RELEASE APPROV 11/9/83		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1 XX ± 030		
	DO NOT SCALE DWG	MODEL NO 21	DWG NO 1100-00-1115 REV F
	SCALE 2/1	CODE IDENT 23338	SHEET 2 OF 2

1100-00-1115 E

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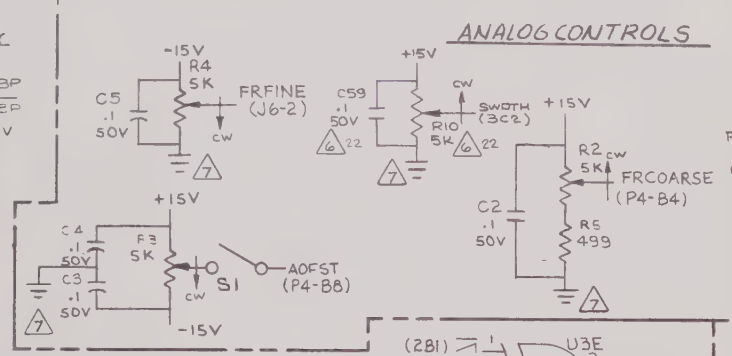
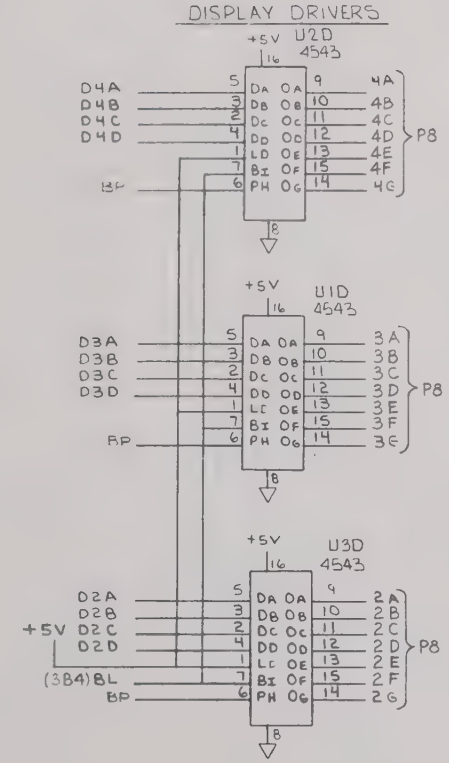
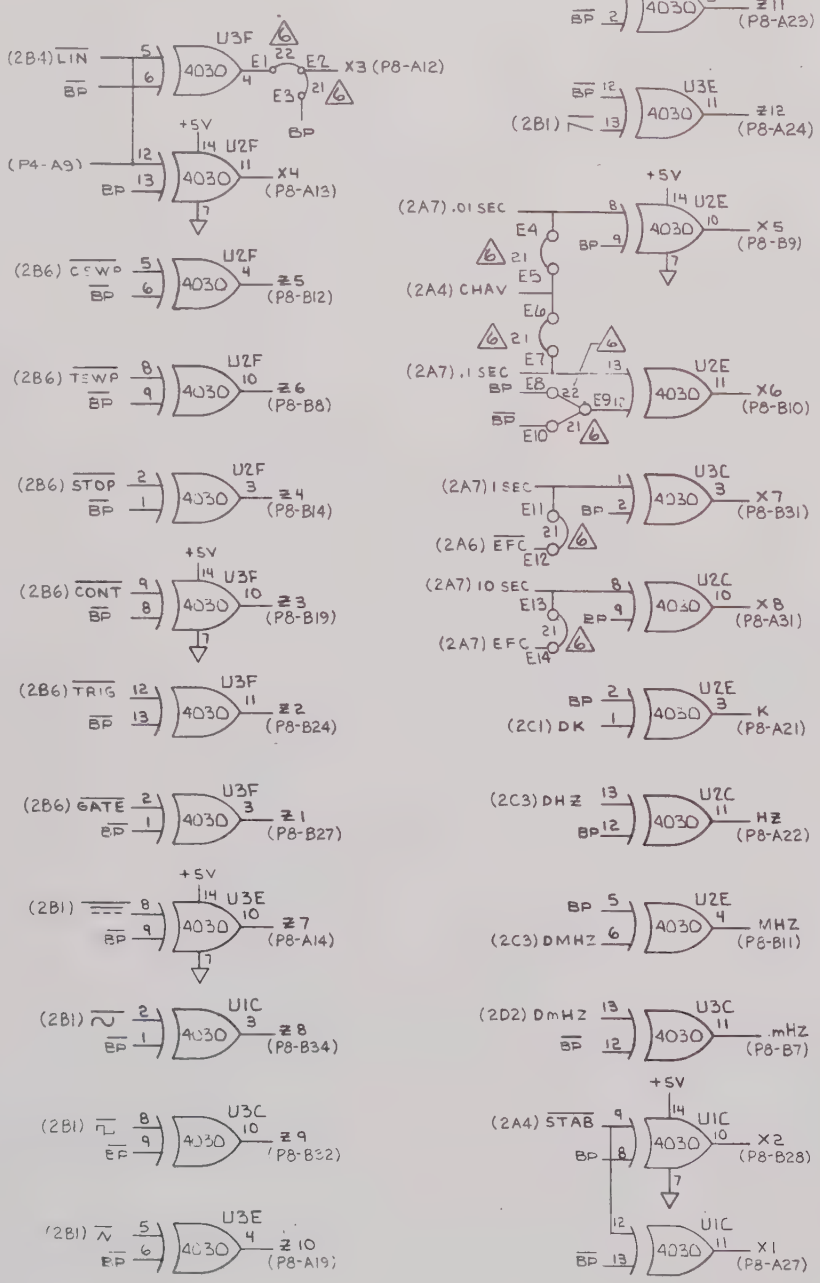
REV	ECN	BY	DATE	APP
D	4601	KA	1-14-88	

ANALOG CONTROLS

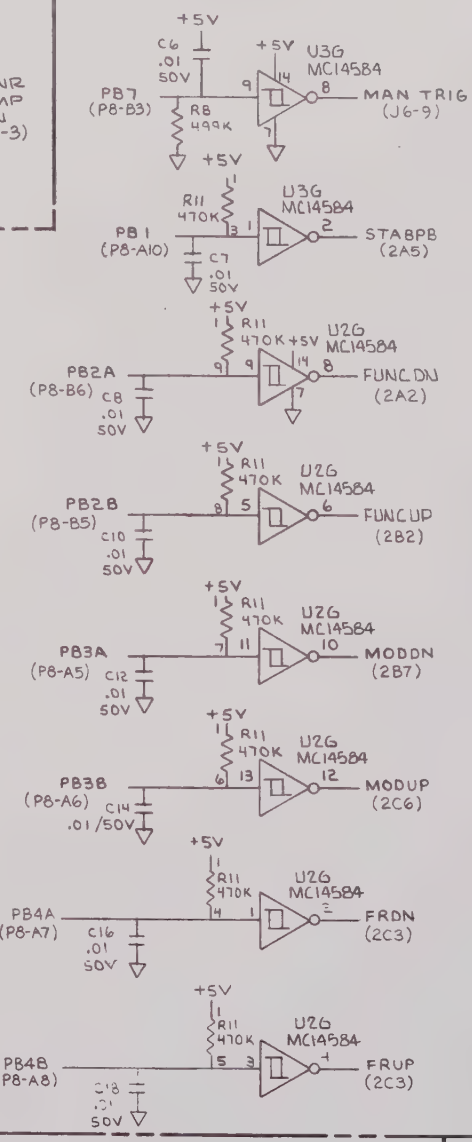


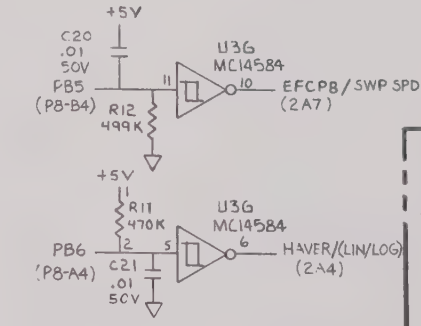
DISPLAY DRIVERS





PUSHBUTTON INTERFACE

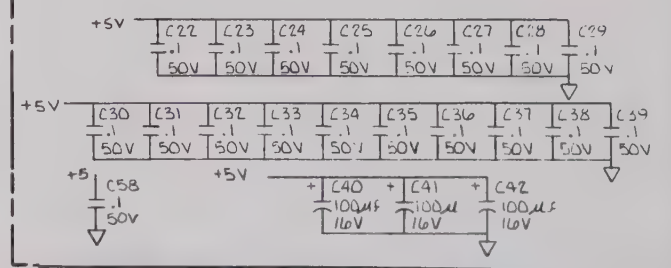




J9
- PREAMP OUT → 1
- PWRAMP IN → 3
- PREAMP GND → 2

P8

+5V	A1	+5V	B1
+5V	A2	+5V	B2
GND	A3	PB7	B3
PB6	A4	PB5	B4
PB3A	A5	PB2B	B5
PB3B	A6	PB2A	B6
PB4A	A7	MHZ	B7
PB4B	A8	Z6	B8
GND	A9	X5	B9
PB1	A10	X6	B10
BP	A11	MHZ	B11
X3	A12	Z5	B12
X4	A13	4B	B13
Z7	A14	Z4	B14
DP1	A15	4A	B15
DP3	A16	4F	B16
4E	A17	4G	B17
4D	A18	3B	B18
Z10	A19	Z3	B19
4C	A20	3A	B20
K	A21	3F	B21
HZ	A22	3G	B22
Z11	A23	2B	B23
Z12	A24	Z2	B24
2F	A25	2A	B25
1B/C	A26	2G	B26
X1	A27	Z1	B27
2E	A28	X2	B28
N/C	A29	N/C	B29
N/C	A30	N/C	B30
X8	A31	X7	B31
3C	A32	Z9	B32
3D	A33	2C	B33
DP2	A34	Z8	B34
3E	A35	2D	B35



9. ANALOG GND SHOWN AS ⏚.
8. LOGIC GND SHOWN AS ⏚.
7. GND REFERENCED TO PREAMP GND ONLY.
6. 21 = MODEL 21 ONLY
   22 = MODEL 22 ONLY
5. "*" INDICATES VALUE IS NOMINAL, SEE PARTS LIST. ACTUAL COMPONENT TO BE SELECTED AT UNIT TEST.
4. CAPACITOR VALUES ARE IN MICROFARADS (µf).
3. RESISTOR VALUES ARE IN OHMS, 1/8 WATT.
2. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111
1. PARTIAL REFERENCE DESIGNATIONS SHOWN. PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A3.

*NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT	DATE 5-1-85	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC STABILIZER CONTROL BOARD (A3)
FINISH WAVETEK PROCESS	RELEASE APPROV 1-14-88		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 21/22	DWG NO 0103-00-1115 REV D
	SCALE	CODE IDENT 23338	SHEET 1 OF 3

0103-00-1115 D

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REV	ECN	BY	DATE	APP

TIMING GENERATION

P4
A1 ← HFSQ
A2 ← MFSQ
A3 ← FRA
A4 ← FR5
A5 ← -15V
A6 ← +5V
A7 ← +5V
A8 ← +15V
A9 ← LIN
A10 ← FRT
B1
B2
B3 ← FR6
B4 ← FRCOARSE
B5
B6
B7 ← ASWP
B8 ← AOFST
B9
B10

Y1 XTAL
C44 20Pf S.M.
C43 75PF S.M.
C45* 470PF S.M.
C46
C47 .01/50V
C48 .01 50V
R14 10K
R15 1.5K
R16 1.5K
R17 10K
R18 6.04K
R19 9.09K
R20 2.49K
U9A 3096
+5V
-15V

50 KHZ (J6-19)
U6B 74HC157
U8A 74HC393
U7A 74HC390
MR (3A7)
U5A 74HC390
U6A 74HC390
U4A 4536
SPD0 (2A8)
SPD1 (2A8)
FRCHG (3C1)
U6B 74HC157
U8D 4049
U5B 74HC107
U7E 4081
CLRCNT (3C3)
MEMCLK (3C5)
GATE (3C6)

MODE CONTROL

J6
1
2 ← FRFINE
3 ← TRIG
4 ← KILL
5 ← VCC KILL
6 ← LOG
7 ← SIN
8 ← TRI
9 ← MAN TRIG
10 ← SQR
11 ← MC1
12 ← MCØ
13 ← SYNTH
14 ← SWP RUN
15 ← FSØ
16 ← EFC
17 ← THAV
18 ← LF
19 ← 50KHZ
20 ← FSI

U4G 74HC193
U5G 4011
MOD UP (1B3)
MOD DN (1C3)
MC1 (J6-11)
U7F 74LS04 (3C1)
SWPT
SWP (3C2)
U4F 74HC138
SWP (3D3) (3B2)
GATE (1B7)
TRIG (1B7)
CONT (1B7)
STOP (1B7)
CSWP (1C7)
TSWP (1C7)
N/C
N/C

SWEEP SPEED CONTROL

U3A 4520
U4C 4555
SPDØ (2B5)
SPD1 (2B5)
10 SEC (1B5)
1 SEC (1B5)
.1SEC (1C5)
.01SEC (1C5)
U4E 74HC10
MCØ (3D3) (J6-12)
U5G 4011
U8E 4011
BL (1B8)

U8C 74HC390
EFCPB/SWPSPD (1D2)
EFC (1B5) (2C1)
U8D 4049

MISC. CONTROL

U4E 74HC10
STAB (3D1)
U8D 4049
CONT (3D2)
U6F 4027
STAB PB (1D3)
(J6-5) VCCKIL
STAB (1A5)
U6G 4012
UNSTAB (3D3)
(1C2) HAVER/(LIN/LOG)
U7A 74HC390
LIN (1C7)
U6C 74LS00
R22 20K
R21 10K
LOG (J6-6)
CHAV (1C5)
U7E 4081
U8E 4011
U8B 74LS04
(J6-17) THAV

FREQUENCY RANGE CONTROL

U6D 74HC42
(1A5) DMHZ
DHZ (1B5)
U5E 4071
(3B8) ÷100
(3A7) MR
U6E 74HC193
FRUP (1B3)
FRDN (1B3)
U5F 4011
FRT (3C8)
U7C 74HC10
DDP2 (1A1)
U7D 74HC10
DDP1 (1A4)
(1A5) D MHZ
U5E 4071
DDP3 (1A4)
U6C 74LS00
FR4 (3C8)
U7C 74HC10
FR5 (3C8)
U7C 74HC10
DK (1B5)
U7D 74HC10
FR6 (3C8)
U6G 4012
U7D 74HC10
LF (J6-18)
U8D 4049
EFC (J6-16)

FUNCTION CONTROL

U5D 74HC193
NC
MR (3A7)
U4D 74HC138
(J6-10) SQR
(1A7) (1A7) (1A7) (1B7)
KILL (J6-4)
(IC5) (ID5)
U4E 74HC10
SYNTH (J6-13)
U5E 4071
TRI (J6-8)
U5E 4071
SIN (J6-7)
U6C 74LS00
FSI (J6-20)
U7E 4081
FSØ (J6-15)
U5F 4011
FUNCUP (1C3)
U5F 4011
FUNCDN (1C3)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT	DATE 5-13-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC STABILIZER CONTROL BOARD (A3)
FINISH WAVETEK PROCESS	RELEASE APPROV 11/4/83		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 21/22	DWG NO 0103-00-1115 REV D
	SCALE	CODE IDENT 23338	SHEET 2 OF 8

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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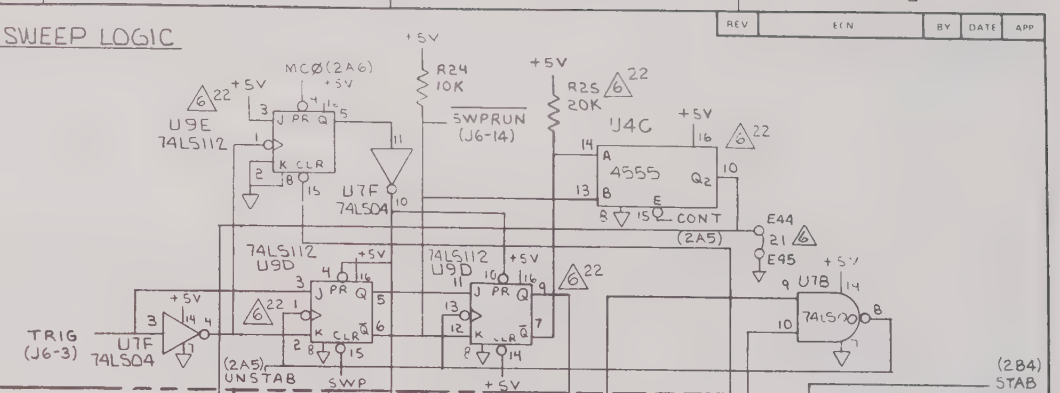
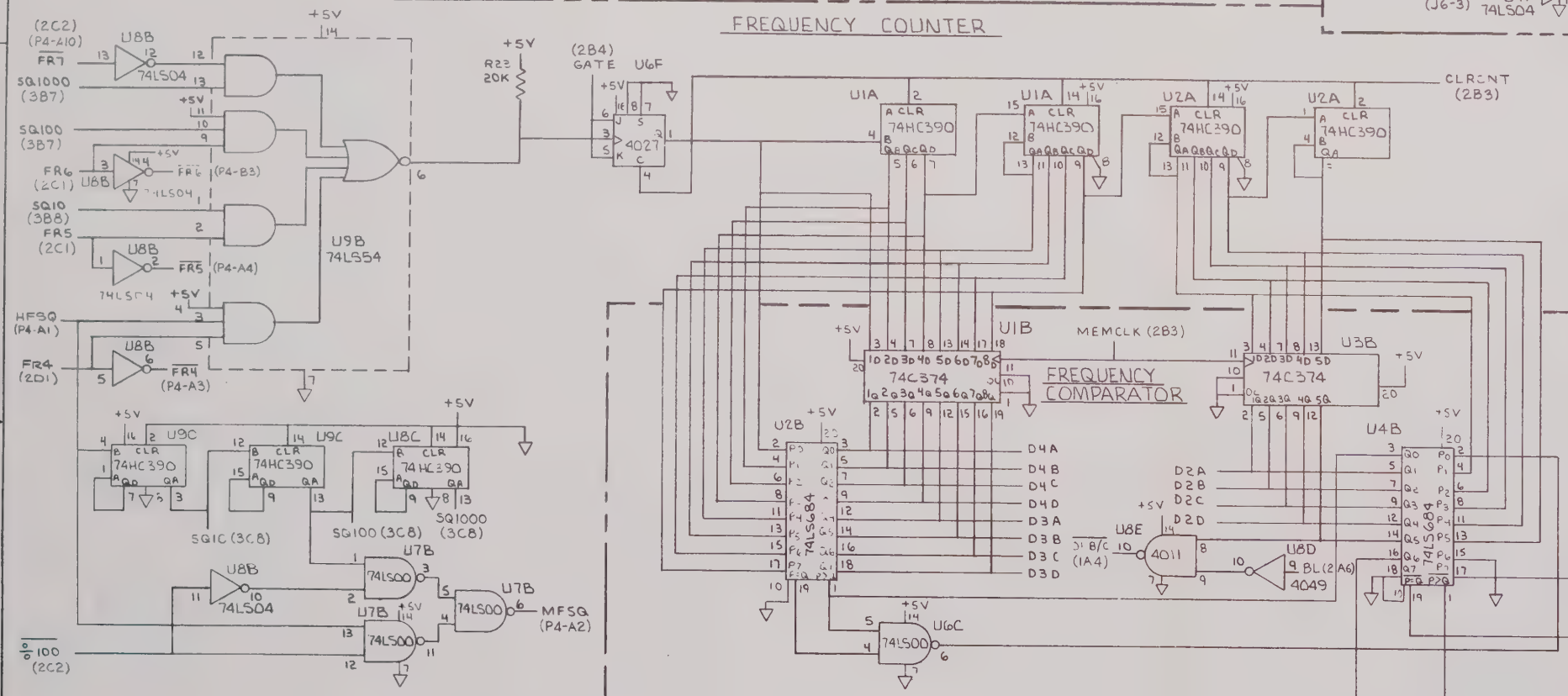
REV	ECN	BY	DATE	APP

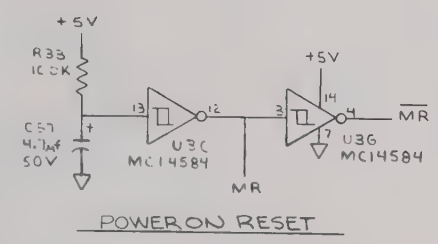
TRIG SWEEP LOGIC



FREQUENCY COUNTER



POWER ON RESET



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC STABILIZER CONTROL BOARD (A3)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 21/22	DWG NO 0103-00-1115 REV
	SCALE	CODE IDENT 23338	SHEET 3 OF 3

0103-00-1115 D

BISHOP GRAPHICS ACCUPRESS REORDER NO A 3094

REV	DESCRIPTION	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, STAB. /CONT	0103-00-1115	WVTK	0103-00-1115	1
C45T	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	1
C1 C10 C12 C14 C16 C18 C20 C21 C47 C48 C6 C7 C8	CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	13
C22 C23 C24 C25 C26 C27 C28 C29 C3 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C4 C5 C54 C55 C58	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	24
C56	CAP, CER, 15PF, 1KV	DD-150	CRL	1500-01-5011	1
C53	CAP, CER, .0015MF, 1KV	DD-152 LONG LEAD	CRL	1500-01-5201	1
C44	CAP, MICA, 20PF, 500V	DM15-200J	ARCO	1500-12-0000	1
C46	CAP, MICA, 470PF, 500V	DM15-471J	ARCO	1500-14-7100	1
C43	CAP, MICA, 75PF, 500V	DM15-750J	ARCO	1500-17-5000	1
C40 C41 C42	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	CRE SERIES 100/25	CAPAR	1500-31-0102	3
C57	CAP, ELECT, 4.7MF/50V RADIAL LEAD, SP .10	CLE SERIES 4.7/50	CAPAR	1500-34-7903	1
1	STAB. /CONTROL BD	21-1115	WVTK	1700-00-1115	1
J9	CONN HEADER 3 PIN	640456-3	AMP	2100-02-0116	1
J6	HEADER, CONN(20 PIN)	643119-1	AMP	2100-02-0151	1

WAVETEK PARTS LIST | TITLE: PCA, STAB. /CONTROL | ASSEMBLY NO. 1100-00-1115 | PAGE: 1 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R11	RES MODULE, 470K	810-1-474-J	TRW	4770-00-0034	1
2	RESISTOR, 0 OHM JUMPER	JPW-02A	ROHM	4799-00-0087	19
3	BUSS WIRE, 22GA	298	ALPHA	6000-92-2000	1
4	SLEEVING, 22GA	TFT-200-22	ALPHA	6001-12-2000	1
U8G	IC	DAC-08EQ	AMD	7000-00-0800	1
U9G	IC, OP-AMP	TL080CP	TI	7000-00-8001	1
U9A	IC	CA-3096AE	RCA	7000-30-9600	1
U5F U5G U8E	IC	CD4011BE	RCA	8000-40-1100	3
U6F	IC, JK FLIP-FLOP	4027B	NSC	8000-40-2700	1
U1C U2C U2E U2F U3C U3E U3F	IC	CD4030AE	RCA	8000-40-3001	7
U5C	IC, MULTIVIBRATOR	4047B	NSC	8000-40-4700	1
U7E	IC	CD4081BE	RCA	8000-40-8100	1
U1D U2D U3D	IC, BCD TO LCD	4543B	NSC	8000-45-4300	3
U6C U7B	IC	74LS00	TI	8000-74-0010	2
U7F U8B	IC	74LS04	TI	8000-74-0410	2
U4E U7C U7D	IC, 3 INPUT NAND	74HC10	MOT	8000-74-1040	3

WAVETEK PARTS LIST | TITLE: PCA, STAB. /CONTROL | ASSEMBLY NO. 1100-00-1115 | PAGE: 3 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Y1	CRYSTAL, 6.4MHZ	VF640	VA-FI	2300-99-0015	1
R6	POT, CONT, 500	4600-01-0109	WVTK	4600-05-0109	1
R2, R4	POT, DUAL, 5K	4600-25-0201	WVTK	4600-25-0201	1
R3	POT, SWITCH, 5K	4602-05-0303	WVTK	4602-05-0303	1
R14 R17 R21 R24	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	4
R33	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	1
R15 R16	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	2
R31	RES, MF, 1/8W, 1%, 178K	RN55D-1783F	TRW	4701-03-1783	1
R22 R23	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	2
R20	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	1
R32	RES, MF, 1/8W, 1%, 2.74K	RN55D-2741F	TRW	4701-03-2741	1
R7	RES, MF, 1.8W, 1%, 46.4	RN55D-46R4F	TRW	4701-03-4649	1
R5	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
R1 R12 R8	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	3
R18	RES, MF, 1/8W, 1%, 6.04K	RN55D-6041F	MEPCO	4701-03-6041	1
R19	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	1
R29 R30	RES, MF, 1/8W, 1%, 90.9K	RN55D-9092F	TRW	4701-03-9092	2

WAVETEK PARTS LIST | TITLE: PCA, STAB. /CONTROL | ASSEMBLY NO. 1100-00-1115 | PAGE: 2 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U6D	IC, 1-OF-10 DECODER	74HC42	MOT	8000-74-4240	1
U9B	IC	74LS54	TI	8000-74-5410	1
U6G	IC	MC14012UBCP	MOT	8001-40-1200	1
U8D	IC	CD4049UBE	RCA	8001-40-4900	1
U5E	IC	MC14071B	MOT	8001-40-7100	1
U2G U3G	IC, SCHMITT TRIGGER	MC14584B	MOT	8001-45-8400	2
U5B	IC, JK FLIP-FLOP	MM74HC107	NSC	8007-41-0740	1
U4D U4F	IC, 1 OF 8 DECODER/ DEMULTIPLEXER	74HC138	MOT	8007-41-3840	2
U8F U9F	IC	SN74LS169BN	TI	8007-41-6911	2
U4G U5D U6E	IC, UP/DOWN COUNTER	MM74HC193	NSC	8007-41-9340	3
U1B U3B	IC	74C374	NAT	8007-43-7430	2
U1A U2A U5A U6A U7A U8C U9C	IC, DECADE COUNTER	MM74HC390	NSC	8007-43-9040	7
U8A	IC, 4-BIT COUNTER	MM74HC393	NSC	8007-43-9340	1
U2B U4B	IC, 8-BIT COMPARATOR	74LS684	TI	8007-46-8410	2

WAVETEK PARTS LIST | TITLE: PCA, STAB. /CONTROL | ASSEMBLY NO. 1100-00-1115 | PAGE: 4 | REV F

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN | DATE | PROJ ENGR | RELEASE APPROV | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030 | DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: PCA STAB/CONTROL

MODEL NO 21 | DWG NO 1100-00-1115 | REV F | CODE IDENT 23338 | SHEET 1 OF 2

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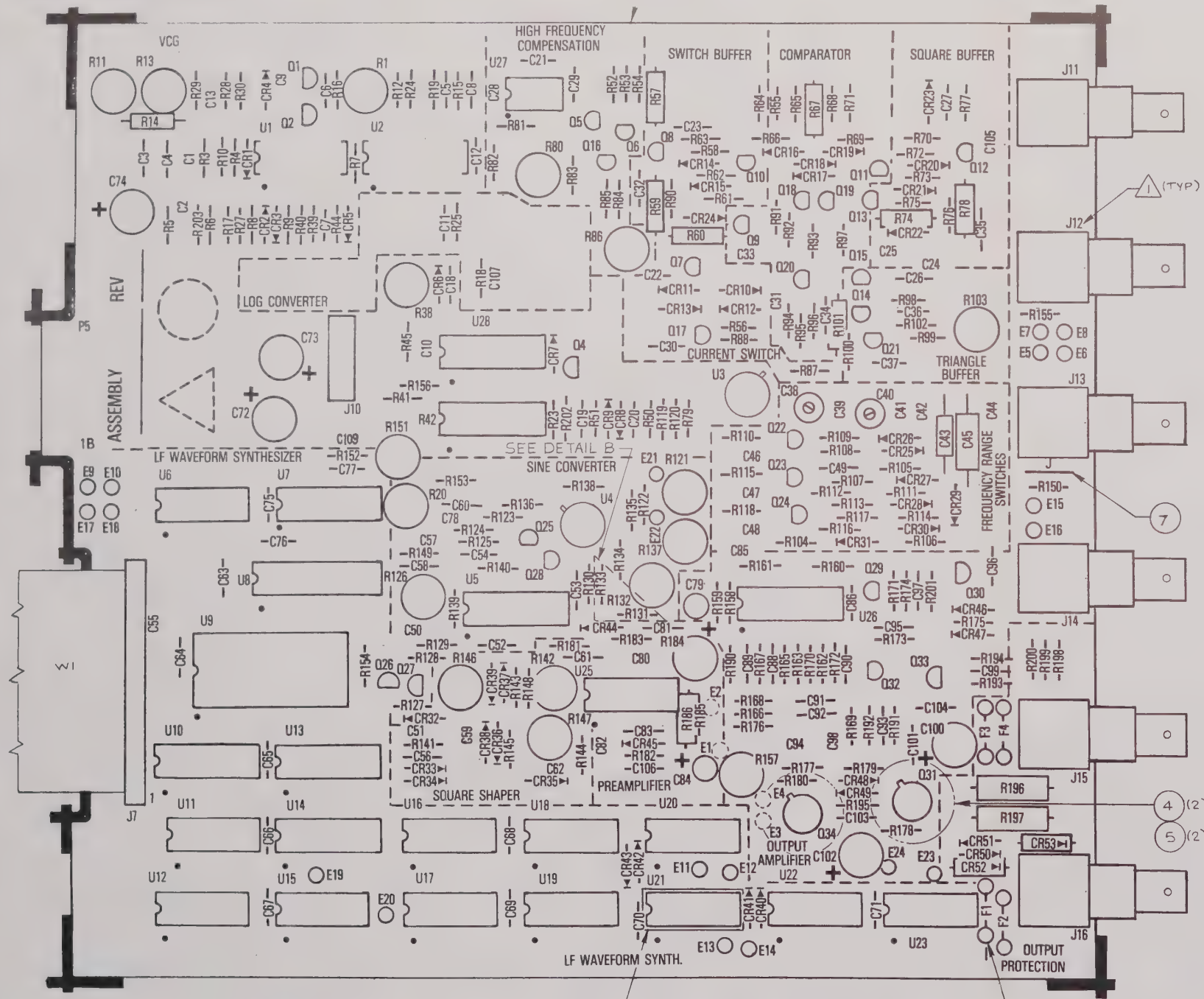
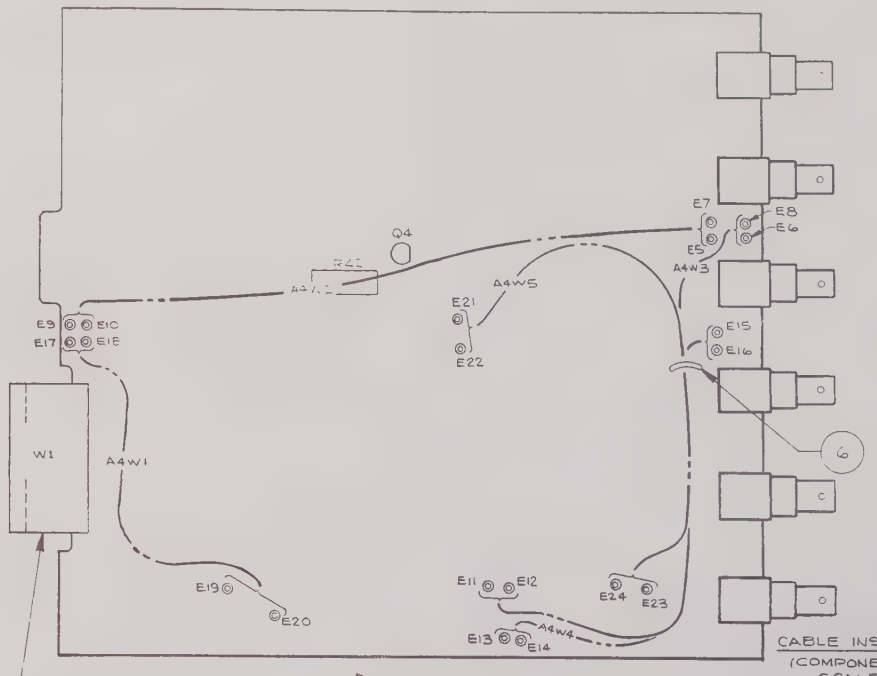
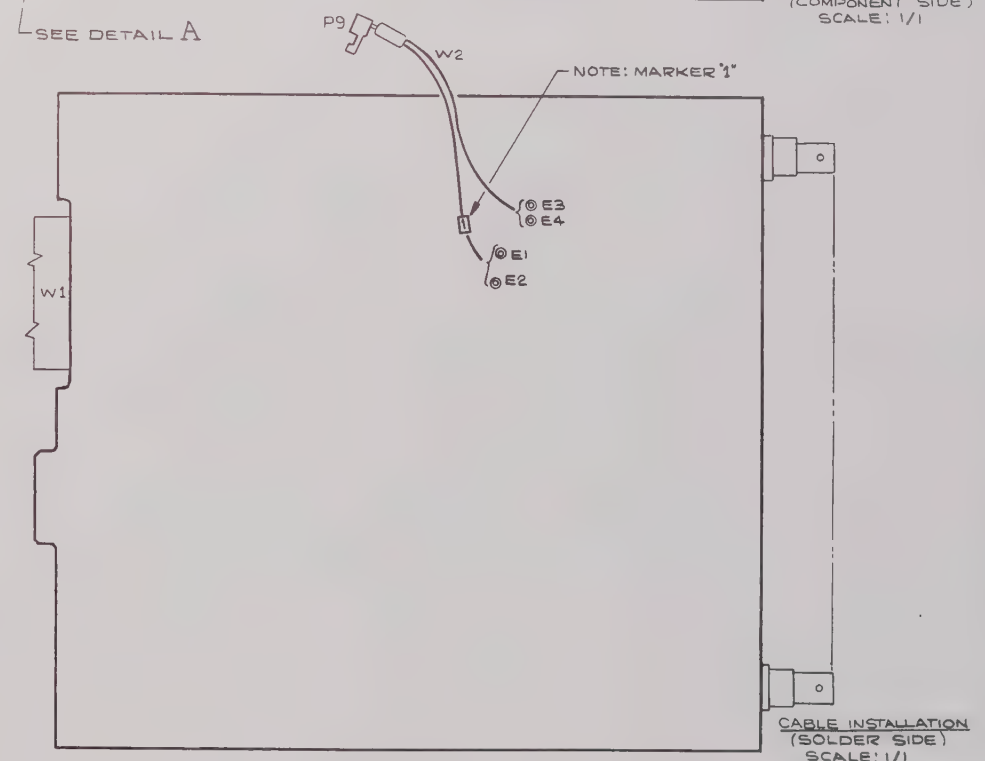
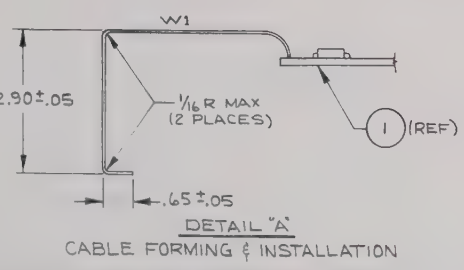




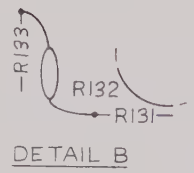




NOTE UNLESS OTHERWISE SPECIFIED

CABLE HOOKUP LIST

REF DES	DESTINATION FROM	DESTINATION TO	REF DES	DESTINATION FROM	DESTINATION TO
A4 W1	E18	E19	A4 W5	E21	E23
	E17	E20		E22	E24
A4 W2	E10	E7	W2	P9-1	E1
	E9	E5		P9-2	E2
A4 W3	E8	E11		P9-3	E3
	E6	E12		P9-2	E4
A4 W4	E16	E13			
	E15	E14			



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 6/26/67	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR		TITLE PCA, WAVEFORM GENERATOR (A4)	
FINISH WAVETEK PROCESS	RELEASE APPROV 11/4/83			
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030			
	DO NOT SCALE DWG		MODEL NO 21	DWG NO 1100-00-1116 REV G
	SCALE 2/1		CODE IDENT 23338	SHEET 3 OF 3

1100-00-1116 : G

B-SHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

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REV	ECN	BY	DATE	APP
C	#4138	[illegible]	1/17/84	
D	#4148	[illegible]	1/31/84	
E	#4194	[illegible]	3/12/84	
F	#4238/...01	KA	7/16/85	
G	#4167	DAM	9/25/85	

VCG

STABILIZER CONT. BD. A3

FRFINE A334 5K CW -15V

FRCOARSE A3R2 5K CW, A3R5 499

POWER SUPPLY BOARD A2A1

ASWP P4 B7 J4 J5 P5 A7 AFREQ B4 B9

J7-2 R203 178K

R3 4.99K R4 4.99K R5 7.5K R6 7.5K

C1 100pf C2 100pf

R7 4.99K

CR1 9.1V 5% IN5239B

R8 7.5K

CR2 1N4148 CR3 1N4148

R9 4.99K

U1 TL084 +15V -15V C3 .1 C4 .1

R10 1M R11 100K CW +15V

VCG ZERO

R13 100K 1100:1 FREQ CW -15V

R14 1M 1/2 W

FS FREQ R1 5K CW

R12 4.75K

C6 .1 R16 2.49K LIN P5-A9

C7 .1 R17 2.49K LOG J7-6

U2 DG211

+15V R19 2.49K R20 100Ω HIGH SYM R42 1K CW R42 1K R23 23.7K

C8 .1 10K R18 C107 330pf

2N3906 Q2

U28 CA3096 AE

+I (2D6)

IN751A 5.1V 10% CR4 C9 470 pf C10 220 pf

Q1 2N3904 R24 2K

U1 TL084

VCG IN J11

+15V -15V

DG211 U2 +5V C12 .1

J7-5 R25 2.49K VCG KILL C11 .1

C13 56 pf R28 4.99K R29 7.5K

SWEEP OUT J13 (22) R26 604

TL084 U1 R27 10K R30 3.01K

J10-14 GCVTST

CW R31 10K HI LOG R32* R33 499

Q3 MP312 R34 4.99K R35 249 R36 500Ω LO LOG CW R37 27.4K -15V

100 pf C14

TL080 U24 C15 .1 C16 470pf C17 .1

LOG CONVERTER MODEL 22 ONLY

R38 100K LOW SYM CW R39 1M R40 1K

VCG TST J10-1 R41 10K R42 1K R42 1K

-I (2B6)

U1 TL084 C18 .1 CR5 IN4148 CR6 7.5V IN755A R44 1K

U28 CA3096AE

U3 CA3019 TRN (2B7)

C5 .1 R15 2.49K FR7 (P5-A10)

HF COMP (2C8) U2 DG11

2N3904 Q4

R45 1K R42 1K R42 1K R42 1K R202 1K R42 1K

CR7 IN4148

C19 .1

RUNTST (J10-8) R156 10K RUN (3A1) C20 .1

+5V R50 2.49K CR8 IN4148 CR9 IN4148 R51 8.25K -15V

8. FOR ASSEMBLY INTERCONNECT SEE INSTRUMENT SCHEMATIC 0004-00-1111.
7. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
6. 21 = MODEL 21 ONLY; 22 = MODEL 22 ONLY
5. "*" INDICATES VALUE IS NOMINAL, SEE PARTS LIST. ACTUAL COMPONENT TO BE SELECTED AT UNIT TEST.
4. CAPACITOR VALUES ARE IN MICROFARADS (μf).
3. RESISTOR VALUES ARE IN OHMS, 1/8 WATT.
2. PARTIAL REFERENCE DESIGNATIONS SHOWN. PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A4.
1. TRANSISTORS HAVE 2800-11-0001 HEATSINK AND 2800-11-0017 TRANSIPAD.

9. "TRIM" INDICATES VALUE SELECTED AT UNIT CALIBRATION.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT	DATE 5-6-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR [illegible]	10-11-83	TITLE SCHEMATIC, WAVEFORM GENERATOR BOARD (A4)
FINISH WAVETEK PROCESS —	RELEASE APPROV [illegible]	11/4/83	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO 21/22	DWG NO 0103-00-1116 REV 6
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-2694

0003-00-0000

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REV	ECN	BY	DATE	APP

GENERATOR LOOP

HIGH FREQUENCY COMP

CURRENT SWITCH · +5V · SWITCH BUFFER · COMPARATOR · SQUARE BUFFER · TRIANGLE BUFFER

+15V · -15V

HF COMP (1B1) · TLO80 U27 · 11MHZ ADJ · R80 2K · R81 1K · C28 470Pf · COMP TST J10-10 · Q5 2N3904 · Q6 2N3906 · +COMP · -COMP · R82 10K · C29 .1 · R83 10K · Q16 2N3904 · R84 1.21K · R85 4.99K · R86 500 CW · TRI BAL · R87 33.2 · R88 6.98K · TRN (1B2)

R52 4.99K · R53 2.87K · R54 2.87K · R56 15.8K · R55 6.98K · C21 .1 · C22 .1 · (IC3) +I · S · Q7 2N5462 · -I (IC3) · C23 .1 · C30 .1 · C31 5Pf · Q8 2N3563 · R57 4.7Ω 1/2W · R58 100 · R59 4.7Ω 1/2W · R60 4.7Ω 1/2W · R61 100 · Q9 2N5771 · CR10 FD777(4) · CR11 · CR12 · CR13 · CR14 1N4148 · CR15 1N4148 · R62 10 · R63 332 · R64 6.19K · Q10 2N5771 · CR16 HP2811 · R65 2K · R66 33.2 · R67 499 1/4 W · R68 2K · CR19 HP2811 · R69 33.2 · Q11 2N5771 · R70 392 · R71 1.78K · R72 100 · Q12 2N3563 · CR20 1N4148 · R73 10 · R74 4.7Ω 1/2W 2N5771 · CR21 1N4148 · R75 100 · Q13 · R76 4.64K · CR22 1N4740 · R77 1K · C105 .001 · C24 5Pf · C25 5Pf · CR17 FD777 · CR18 FD777 · CR23 1N9598 · C26 .1 · C27 .1

U3 CA3019 · Q18 2N3563 · Q19 2N3563 · C33 330 Pf 8M · R91 3.01K · R92 332 · R97 332 · CR24 1N4740A · R90 2.49K · C32 .1 · Q17 2N5485 · R93 100 · Q20 2N3563 · R94 1.1K · R95 10.5K · R96 4.32K · C34 .1 · C35 .1 · R98 4.99K · C36 .1 · R99 10K · R100 10 · R103 10K CW · R102 1K · Q21 2N3904 · C37 .1 · R101 1K 1/4W · Q14 2N5485 · Q15 2N3563 · R79 10K

E5 · E9 · A4W2 · E7 · E10 · A4 · HFSQ P5-A1 · E8 · E11 · A4W3 · E6 · E12 · HFSQ (3B4) · TRITST J10-3 · TR8 (3D8)

BASELINE ADJ.

C38 3.5-13 pf · C39 TRIM · 1MHZ ADJ · 1.1MHZ ADJ · C40 7-35 Pf · C41 * (5) · C42 330Pf SM · C43 .0047 1% MYLAR · C44 * (5) · C45 .047 1% MYLAR · CR31 1N4148 · +5V

R104 4.64K · Q22 2N3906 · R110 2.21K · FR6 P5-B3 · C46 .001 · R108 90.9 · CR25 IN5282 · R105 10M 1/4W · R106 7.5K · R107 7.5K · CR26 IN5282 · R109 20K · R111 10M 1/4W · C49 .1 · Q23 2N3906 · R115 2.21K · FR5 P5-A4 · C47 .001 · R112 90.9 · CR28 IN5282 · CR27 IN5282 · R113 20K · R114 10M 1/4W · CR29 IN5282 · Q24 2N3906 · R118 2.21K · FR4 P5-A3 · C48 .001 · R116 90.9 · CR30 IN5282 · R117 20K

FREQUENCY RANGE SWITCHES

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT	DATE 5-9-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR	6-14-83	TITLE SCHEMATIC, WAVEFORM GENERATOR BOARD (A4)
FINISH WAVETEK PROCESS —	RELEASE APPROV	11/9/83	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 21/22 · DWG NO 0103-00-1116 · REV G
	SCALE NONE		CODE IDENT 23338 · SHEET 2 OF 4

0103-00-1116 G

BISHOP GRAPHICS ACCUPRESS REORDER NO. A-3804

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REV	ECN	BY	DATE	APP

FUNCTION SELECT

SINE CONVERTER

TRB (2C2) → R120 182 → R121 200 CW SIN DISTA; R119 100; R122 1K 50K THERMISTOR

CR32 +5V → Q25 2N3906; R123 4.64K; R124 6.98K

C110 TRIM 33PF; R133 29.9K; R131 150; SINUSOIDAL RISE COR CW; CA3019 U4

R135 150; CW R137 500 SIN DISTC; R136 33.2K; R138 24.9K

R134 27.4 → U5 DG211 (Q28 2N5771; C53 .1; C54 .1; R140 2.49K; +15V; -15V)

SIN J7-7; TRI J7-8

R125 10K; R127 4.64K; Q26 2N3906; R128 6.98K; Q27 2N5771; R139 2.49K; C51 .001; C52 .1; U5 DG211

CW R126 200 TRI LEVEL; R129 681; C50 TRIM (9)

MFSQ (2D2) → A4W1 E18 E19 E17 E20

SQUARE SHAPER

TTL SQ (3B2) → R141 2K; SQR UPPER CW R142 5K; R143 12.1K; CR33 IN4148; CR34 IN4148; CR35 IN4148; C56 .1

CR36 FD777; CR37 FD777; CR38 FD777; CR39 FD777; U5 DG211; R146 1K PEAKING ADJ CW; C59 33pf

R144 4.99K; R145 12.1K; R147 5K CW; SQR LOWER; C60 .1; C61 .1; R148 2.49K; J7-10 SQR (3B2); C62 .001

SYNTH SIG (3A7) → C57 .001; R149 2.49K; U5 DG211; C58 .1; SYNTH J7-13

TO PREAMPLIFIER (4B8); +15V; +5V

P5 CARD EDGE TO PWR SUPPLY

A1 → HFSQ	B1 → GND
A2 → MFSQ	B2 → GND
A3 → $\overline{FR4}$	B3 → $\overline{FR6}$
A4 → $\overline{FR5}$	B4 → AFREQ
A5 → -15V	B5 → GND
A6 → +5V	B6 → GND
A7 → ASWP	B7 → GND
A8 → +15V	B8 → AOFST
A9 → $\overline{LIN}$	B9 → GND
A10 → $\overline{FR7}$	B10 → GND

J11 → VCG IN
J12 → TRIG IN
J13 → EXT REF MOD.21 SWP OUT MOD.22
J14 → SYNC OUT
J15 → FUNCOUT (-20 dB)
J16 → FUNCOUT (50Ω)

PC MOUNTING BNC

J10 TEST CONNECTOR

1	VCG TST
2	GND
3	TRI TST
4	GND
5	-15V
6	+5V
7	+15V
8	RUN TST
9	FUNC TST
10	COMP TST
11	GND
12	N.C.
13	GND
14	GCV TST

+5V → C63 .1; C64 .1; C65 .1; C66 .1; C67 .1; C68 .1; C69 .1; C70 .1; C71 .1; C72 47µf 50V; +15V C74 100µf 25V; C73 100µf 25V; -15

LF WAVEFORM SYNTHESIZER

EFC J7-16 → U15 74LS00; U15 74LS00; U19 74LS04

+5V CR40 IN4148; R150 10K; REF IN (21) J13; U21 74LS04; U21 74LS04; CR41 IN4148

U6 74LS107; U11 74LS86; U12 74LS08; FSO J7-15

LF LEVEL CW +15V R151 500; R152 6.81K; C109 100pf; R153 13.7K

U8 DAC-08; U9 2716; FS1 J7-20; C75 .01; C76 .1; C77 .1; C78 .0022; R154 3.01K; SYNTH SIG (3D5)

U11 74LS86; U14 74LS169 U/D A B C D QA QB QC QD; NC

U12 74LS08; U10 74LS169; U19 74LS04; U18 74LS02; U16 74F11

U17 74F74; U13 74LS133; TRIG IN J12; R155 15K

THAV J7-17; MAN TRIG J7-9; J7-11 MC1; J7-12 MCØ; J7-3 TRIG CR42 IN4148; CR43 IN4148

SQUARE SELECTOR

HFSQ (2D2) → U20 74LS00; U19 74LS04; U20 74LS00; U21 74LS04; U21 74LS04; A4W4 E13 E14 E15 E16 J14 SYNC OUT

U16 74F11; TTL SQ (3C5); U19 74LS04 SQR (3C4)

LF J7-18; U20 74LS00; U17 74F74

SWP RUN J7-14; U22 74F00; U23 74F74; A4W5 E23 E21 E24 E22 RUN (1A3) (1A3)

KILL J7-4; U22 74F00

U12 74LS08; U15 74LS00; U23 74F74

TRIGGER LOGIC

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT	DATE 5-11-83	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL //	PROJ ENGR	6-14-83	TITLE SCHEMATIC, WAVEFORM GENERATOR BOARD (A4)	
FINISH WAVETEK PROCESS //	RELEASE APPROV	11/4/83		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		MODEL NO 21/22	DWG NO 0103-00-1116 REV 6
	DO NOT SCALE DWG		CODE IDENT 23338	SHEET 3 OF 4
	SCALE NONE			

0103-00-1116 G

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3384

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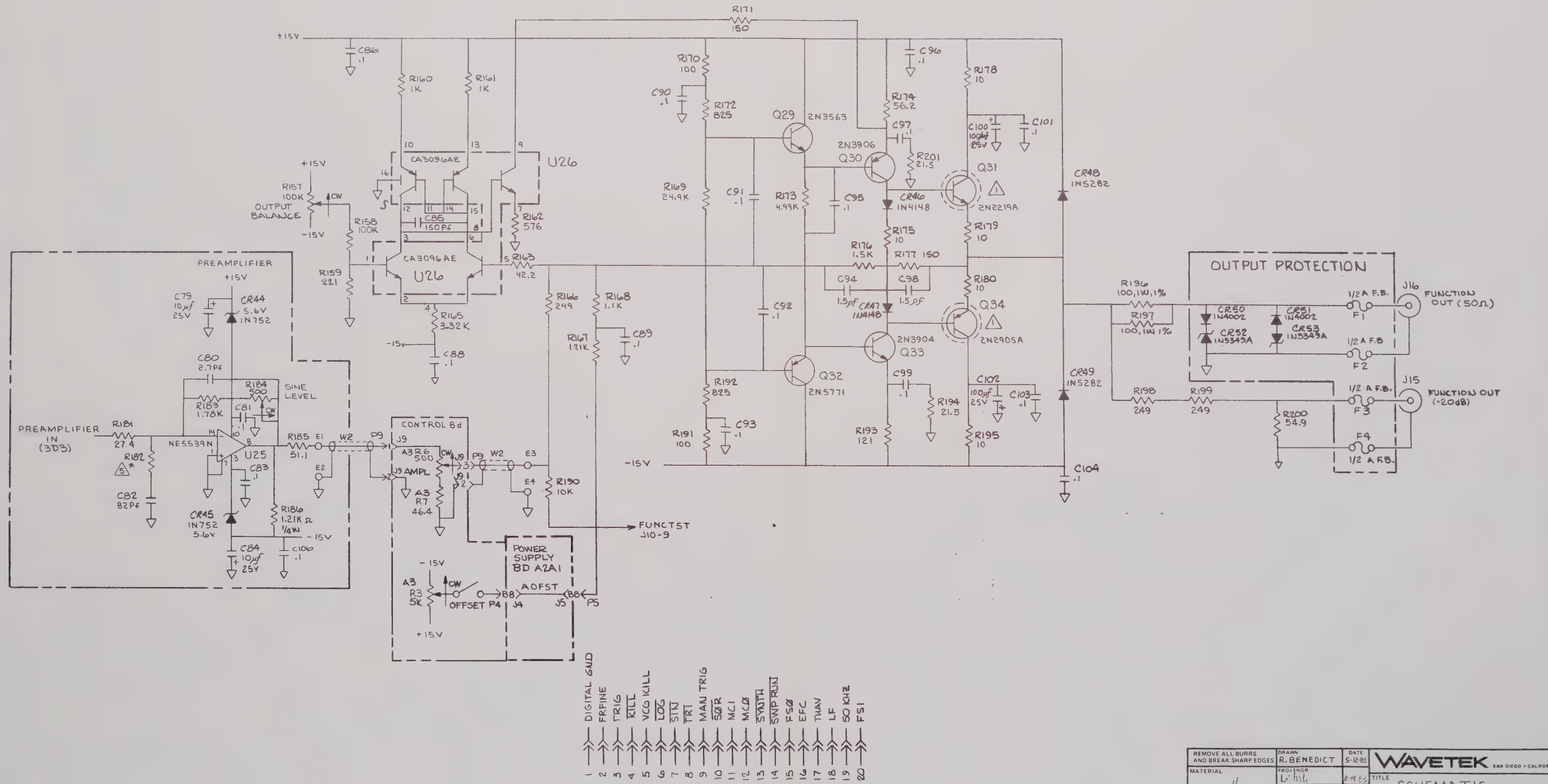
REV	ECN	BY	DATE	APP

OUTPUT AMPLIFIER



RIBBON CONNECTOR TO CONTROL BOARD J7

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. BENEDICT	DATE 5-12-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR		TITLE SCHEMATIC, WAVEFORM GENERATOR BOARD (A4)
FINISH WAVETEK PROCESS —	RELEASE APPROV 11/4/83		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 2112	DWG NO 0103-00-1116 REV G
	SCALE NONE	CODE IDENT 23338	SHEET 4 OF 4

0103-00-1116 G

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3884

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	SCHEMATIC, WAVE/GEN	0103-00-1116	WVTK	0103-00-1116	1
C24 C25 C31	CAP, CER, 5PF, 1KV	DD-050	CRL	1500-00-5011	3
C1 C109 C2	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	3
C105 C44T C46 C47 C48 C51 C55 C57 C62	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-0211	9
C75	CAP, CER, MN, .01MF, 50V	QE50-103ZA	MURAT	1500-01-0310	1
C101 C103 C104 C106 C11 C12 C18 C19 C20 C21 C22 C23 C26 C27 C29 C3 C30 C32 C34 C35 C36 C37 C4 C49 C5 C52 C53 C54 C56 C58 C6 C60 C61 C63 C64 C65 C66 C67 C68 C69 C7 C70 C71 C76 C77 C8 C81 C83 C86 C88 C89 C90 C91 C92 C93 C95 C96 C97 C99	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z030A	CORNG	1500-01-0405	59
C85	CAP, CER, 130PF, 1KV	DD-131	CRL	1500-01-5111	1
C94 C98	CAP, CER, 1.5PF, 1KV	10TCC-V15	SPRAG	1500-01-5507	2
C10	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	1
C78	CAP, CER, .0022, 1KV	DD-222SLL	CRL	1500-02-2201	1
C80	CAP, CER, MN, 2.7PF, 50V	IMCAC2R7D	ARCO	1500-02-7505	1
C110T	CAP, CER, 33PF, 1KV	DD-330 LONG LEAD	CRL	1500-03-3001	1

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN | ASSEMBLY NO. 1100-00-1116 | REV | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C59	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	1
C107	CAP, CER, 330PF, 1KV	DD-331	CRL	1500-03-3111	1
C28 C9	CAP, CER, 470PF, 1KV	DD-471	CRL	1500-04-7111	2
C13	CAP, CER, 56PF, 1KV	DD-560	CRL	1500-05-6001	1
C82	CAP, CER, 82PF, 1KV	DD-820	CRL	1500-08-2011	1
C33 C42	CAP, MICA, 330PF, 500V	DM15-331J	ARCO	1500-13-3100	2
C41T	CAP, MICA, 82PF, 500V	DM15-820J	ARCO	1500-18-2000	1
C79 C84	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	CRE SERIES 10/25	CAPAR	1500-31-0002	2
C100 C102 C73 C74	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	4
C72	CAP, ELECT, 47MF, 50V RADIAL LEAD, SP .20	ULB1J470M	NICH	1500-34-7003	1
C43	CAP, MYLR, .0047MF, 50V	C5R472F	ELPAC	1500-44-7203	1
C45	CAP, MYLR, .047MF, 50V	C5R473F	ELPAC	1500-44-7303	1
C38	VARI, 3.5-13PF, 250V	7S-TRIKO-02 3.5/13PF	TRIKO	1500-51-3000	1
C40	VARI, 7-35PF, 250V	7S-TRIKO-02 7/35 PF	TRIKO	1500-53-5000	1
1	WAVEFORM GEN BD	21-1116	WVTK	1700-00-1116	1

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN | ASSEMBLY NO. 1100-00-1116 | REV | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
J11 J12 J13 J14 J15 J16	CONNECTOR, BNC(PC)	227161-1	AMP	2100-01-0019	6
2	SKT, IC, 14 PIN	DILB14P/10B	BURND	2100-03-0066	1
3	TERM	2000B1	USECO	2100-05-0009	8
J10	HEADER, 14 PIN, 2X7	CA-D14RSP100-230-090	CA	2100-05-0053	1
F1 F2 F3 F4	FUSE, 1/2A, 125V(PC)	255.500	LITFU	2400-05-0035	4
4	HEAT SINK	207	WAKE	2800-11-0001	2
5	TRANSIPAD	333-125-NY	BLINN	2800-11-0017	2
6	MOUSETAIL	2829-75-2	RUBTK	2800-12-0005	1
R20	POT, TRIM, 100	91AR100	BECK	4600-01-0103	1
R146	POT, TRIM, 1K	91AR1K	BECK	4600-01-0209	1
R103	POT, TRIM, 10K	91AR10K	BECK	4600-01-0315	1
R11 R13 R157 R38	POT, TRIM, 100K	91AR100K	BECK	4600-01-0402	4
R121 R126	POT, TRIM, 200	91AR200	BECK	4600-02-0101	2
R80	POT, TRIM, 2K	91AR2K	BECK	4600-02-0201	1
R132 R137 R151 R184 R86	POT, TRIM, 500	91AR500	BECK	4600-03-0104	5
R1 R142 R147	POT, TRIM, 5K	91AR5K	BECK	4600-03-0203	3
R57 R59 R60 R74 R78	RES, C, 1/2W, 5%, 4.7	RC-1/2-4R7J	STKPL	4700-25-0479	5

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN | ASSEMBLY NO. 1100-00-1116 | REV | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R14	RES, C, 1/2W, 5%, 1M	RC-1/2-105J	STKPL	4700-25-1004	1
R119 R170 R191 R58 R61 R72 R75 R93	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	8
R102 R160 R161 R202 R40 R44 R45 R77 R81	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	9
R125 R150 R156 R18 R190 R27 R41 R79 R82 R83 R99	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	11
R158	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	1
R10 R39	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	2
R100 R175 R178 R179 R180 R195 R62 R73	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	8
R95	RES, MF, 1/8W, 1%, 10.5K	RN55D-1052F	TRW	4701-03-1052	1
R168 R94	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	2
R193	RES, MF, 1/8W, 1%, 121	RN55D-1210F	TRW	4701-03-1210	1
R167 R84	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	2
R143 R145	RES, MF, 1/8W, 1%, 12.1K	RN55D-1212F	TRW	4701-03-1212	2
R153	RES, MF, 1/8W, 1%, 13.7K	RN55D-1372F	TRW	4701-03-1372	1
R131 R135 R171 R177	RES, MF, 1/8W, 1%, 130	RN55D-1300F	TRW	4701-03-1300	4

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN | ASSEMBLY NO. 1100-00-1116 | REV | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R176	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	1
R155	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	1
R36	RES, MF, 1/8W, 1%, 15.8K	RN55D-1582F	TRW	4701-03-1582	1
R183 R71	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	2
R203	RES, MF, 1/8W, 1%, 178K	RN55D-1783F	TRW	4701-03-1783	1
R120	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1
R141 R24 R65 R68	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	4
R109 R113 R117	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	3
R194 R201	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	2
R159	RES, MF, 1/8W, 1%, 221	RN55D-2210F	TRW	4701-03-2210	1
R110 R115 R118	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	3
R23	RES, MF, 1/8W, 1%, 23.7K	RN55D-2372F	TRW	4701-03-2372	1
R166 R198 R199	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	3
R139 R140 R148 R149 R15 R16 R17 R19 R25 R50 R90	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	11
R133 R138 R169	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	3
R134 R181	RES, MF, 1/8W, 1%, 27.4	RN55D-27R4F	TRW	4701-03-2749	2

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN | ASSEMBLY NO. 1100-00-1116 | REV | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R53 R54	RES, MF, 1/8W, 1%, 2.87K	RN55D-2871F	TRW	4701-03-2871	2
R154 R30 R91	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	3
R63 R92 R97	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	3
R165	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R130 R136	RES, MF, 1/8W, 1%, 33.2K	RN55D-3322F	TRW	4701-03-3322	2
R66 R69 R87	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	3
R70	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R163	RES, MF, 1/8W, 1%, 42.2	RN55D-42R2F	TRW	4701-03-4229	1
R96	RES, MF, 1/8W, 1%, 4.32K	RN55D-4321F	TRW	4701-03-4321	1
R104 R123 R127 R76	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	4
R12	RES, MF, 1/8W, 1%, 4.75K	RN55D-4751F	TRW	4701-03-4751	1
R144 R173 R28 R3 R4 R52 R7 R85 R9 R98	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	10
R182T R185	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	2
R200	RES, MF, 1/8W, 1%, 54.9	RN55D-54R9F	TRW	4701-03-5499	1
R174	RES, MF, 1/8W, 1%, 56.2	RN55D-56R2F	TRW	4701-03-5629	1
R162	RES, MF, 1/8W, 1%, 576	RN55D-5760F	TRW	4701-03-5760	1

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN | ASSEMBLY NO. 1100-00-1116 | REV | PAGE 6

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PCA WAVEFORM GENERATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO 21
	DO NOT SCALE DWG		DWG NO 1100-00-1116 REV G
	SCALE		CODE IDENT 23338 SHEET 1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R64	RES, MF, 1/8W, 1%, 6.19K	RN55D-6191F	TRW	4701-03-6191	1
R129	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	1
R152	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	1
R124 R128 R55 R88	RES, MF, 1/8W, 1%, 6.98K	RN55D-6981F	TRW	4701-03-6981	4
R106 R107 R29 R5 R6 R8	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	6
R172 R192	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	2
R51	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1
R108 R112 R116	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	3
R101	RES, MF, 1/4W, 1%, 1K	RN60D1001F	TRW	4701-13-1001	1
R186	RES, MF, 1/4W, 1%, 1.21K	RN60D-1211F	TRW	4701-13-1211	1
R67	RES, MF, 1/4W, 1%, 499	RN60D4990F	TRW	4701-13-4990	1
R196 R197	RES, MF, 1W, 1%, 100	RN70D-1000F	TRW	4701-33-1000	2
R42	RES MODULE	4116R-001-102	BOURN	4770-00-0019	1
R105 R111 R114	RES, MF, 1/4W, 1%, 10M	CC1005F	AB	4799-00-0056	3
7	RESISTOR, 0 OHM JUMPER	JP02T680	ROHM	4799-00-0087	1
CR4	DIODE	1N751A	FAIR	4801-01-0751	1

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN | ASSEMBLY NO. 1100-00-1116 | REV

PAGE 7

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q1 Q16 Q21 Q33 Q4 Q5	TRANS	2N3904	FAIR	4901-03-9040	6
Q2 Q22 Q23 Q24 Q25 Q26 Q30 Q6	TRANS	2N3906	FAIR	4901-03-9060	8
Q7	TRANS	2N5462	MOT	4901-05-4620	1
Q14 Q17	TRANS	2N5485	MOT	4901-05-4850	2
Q10 Q11 Q13 Q27 Q28 Q32 Q9	TRANS	2N5771	NSC	4901-05-7710	7
R122	THERMISTER	1K-501-K	MCI	5300-00-0011	1
W1	CABLE, FLEX CIRCUIT	1-86947-9	AMP	6001-60-0005	1
U7	IC	DAC-08EQ	AMD	7000-00-0800	1
U27	IC, OP-AMP	TL080CP	TI	7000-00-8001	1
U1	IC	TL084CN	TI	7000-00-8400	1
U3 U4	IC	CA-3019	RCA	7000-30-1900	2
U26 U28	IC	CA-3096AE	RCA	7000-30-9600	2
U25	IC, OP AMP	NE5539	SIG	7000-55-3900	1
U2 U5	IC, QUAD SPST CMOS ANALOG SWITCH	DG211CJ	SILX	8000-02-1100	2
U22	IC, QUAD 2-INPUT NAND GATE	74F00	FAIR	8000-74-0002	1

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN | ASSEMBLY NO. 1100-00-1116 | REV

PAGE 9

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR44 CR45	DIODE, ZENER	1N 752A	MOT	4801-01-0752	2
CR6	DIODE, ZENER, 7.5V	1N755A	MOT	4801-01-0755	1
CR23	DIODE	1N959	SIEM	4801-01-0959	1
CR22 CR24	DIODE	1N4740A	MOT	4801-01-4740	2
CR1	DIODE	1N5239	TEL	4801-01-5239	1
CR25 CR26 CR27 CR28 CR29 CR30 CR48 CR49	DIODE	1N5282	FAIR	4801-01-5282	8
CR52 CR53	DIODE	1N5349A	MOT	4801-01-5349	2
CR50 CR51	DIODE	1N4002	FAIR	4801-02-0001	2
CR10 CR11 CR12 CR13 CR17 CR18 CR36 CR37 CR38 CR39	DIODE	FD777	FAIR	4807-02-0777	10
CR14 CR15 CR2 CR20 CR21 CR3 CR31 CR32 CR33 CR34 CR35 CR40 CR41 CR42 CR43 CR46 CR47 CR5 CR7 CR8 CR9	DIODE	1N4148	FAIR	4807-02-6666	21
CR16 CR19	DIODE	5082-2811	HP	4809-02-2811	2
Q31	TRANS	2N2219A	NSC	4901-02-2191	1
Q34	TRANS	2N2905A	NSC	4901-02-9051	1
Q12 Q15 Q18 Q19 Q20 Q29 Q8	TRANS	2N3563	FAIR	4901-03-5630	7

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN | ASSEMBLY NO. 1100-00-1116 | REV

PAGE 8

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U15 U20	IC	74LS00	TI	8000-74-0010	2
U18	IC	74LS02	TI	8000-74-0210	1
U19 U21	IC	74LS04	TI	8000-74-0410	2
U12	IC	74LS08	TI	8000-74-0810	1
U16	IC, 3-INPUT AND	74F11	FAIR	8000-74-1102	1
U17 U23	IC, DUAL D-TYPE FLIP-FLOP	74F74	FAIR	8000-74-7402	2
U11	IC	74LS86	TI	8000-74-8610	1
U6	IC	74LS107A	TI	8007-41-0710	1
U13	IC, 13-INPUT NAND	74LS133	FAIR	8007-41-3310	1
U10 U14	IC	SN74LS169BN	TI	8007-41-6911	2
U8	IC	74LS374	TI	8007-43-7410	1
U9	IC, PROGRAMMED REF: 8000-27-1600	8600-00-0249	WVTK	8600-00-0249	1

WAVETEK PARTS LIST | TITLE: PCA, WAVEFORM GEN | ASSEMBLY NO. 1100-00-1116 | REV

PAGE 10

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PCA WAVEFORM GENERATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 21 / DWG NO 1100-00-1116 / REV G
	SCALE		CUST IDENT 23338 / SHEET 2 OF 2

BISHOP GRAPHICS INC EXPRESS REORDER NO A27086

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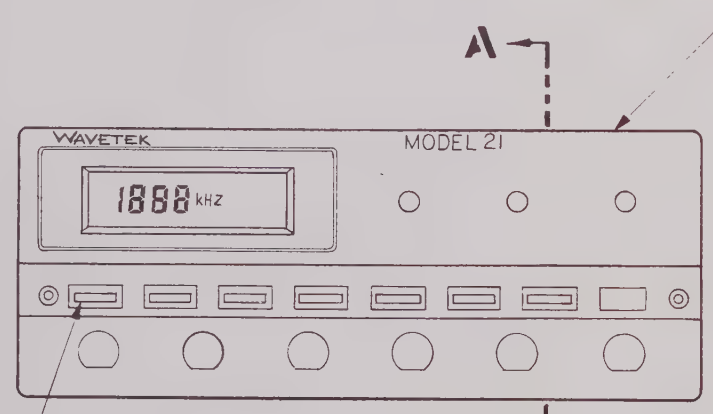
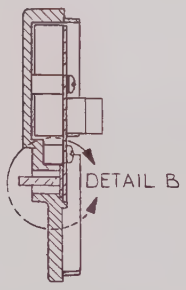
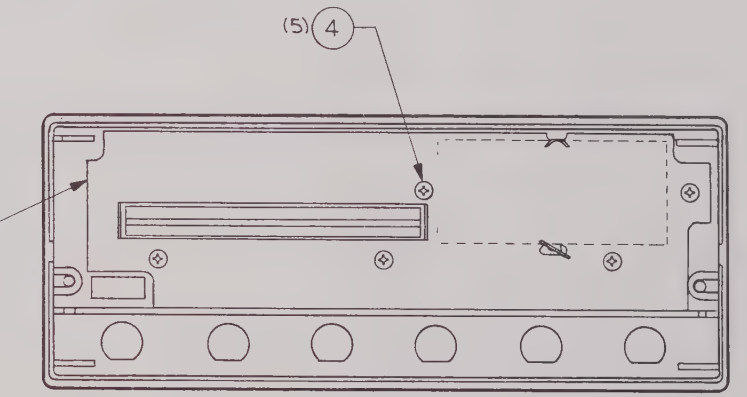
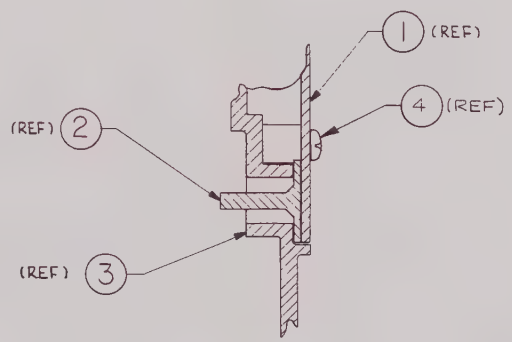
REV	ECN	BY	DATE	APP
A	→ 4492		6-9-83	





SECTION A-A





DETAIL B
SCALE 2:1

REFERENCE DESIGNATORS	PART DESCRIPTION	DRIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCA, DISPLAY	21-1117	WVTK	1208-00-1117	1
2	KEY PAD STRIP	1400-01-6230	WVTK	1400-01-6230	1
3	FRONT, HOUSING (MODEL 21)	1400-01-6250	WVTK	1400-01-6250	1
4	SCREW, SELF TAPPING TYPE B, P.H. CROSS RECESS, 4-40X1/4	4-24 X 1/4	CMRCL	2800-22-4142	5

1. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.MAGNOLIA	DATE 6-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: ASSEMBLY FRONT PANEL MODEL 21 (A1)
	RELEASE APPROV	7-4-83	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 21 / DWG NO 1101-00-1112 / REV A
	SCALE FULL		CODE IDENT 23338 / SHEET 1 OF 1

1101-00-1112 A

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

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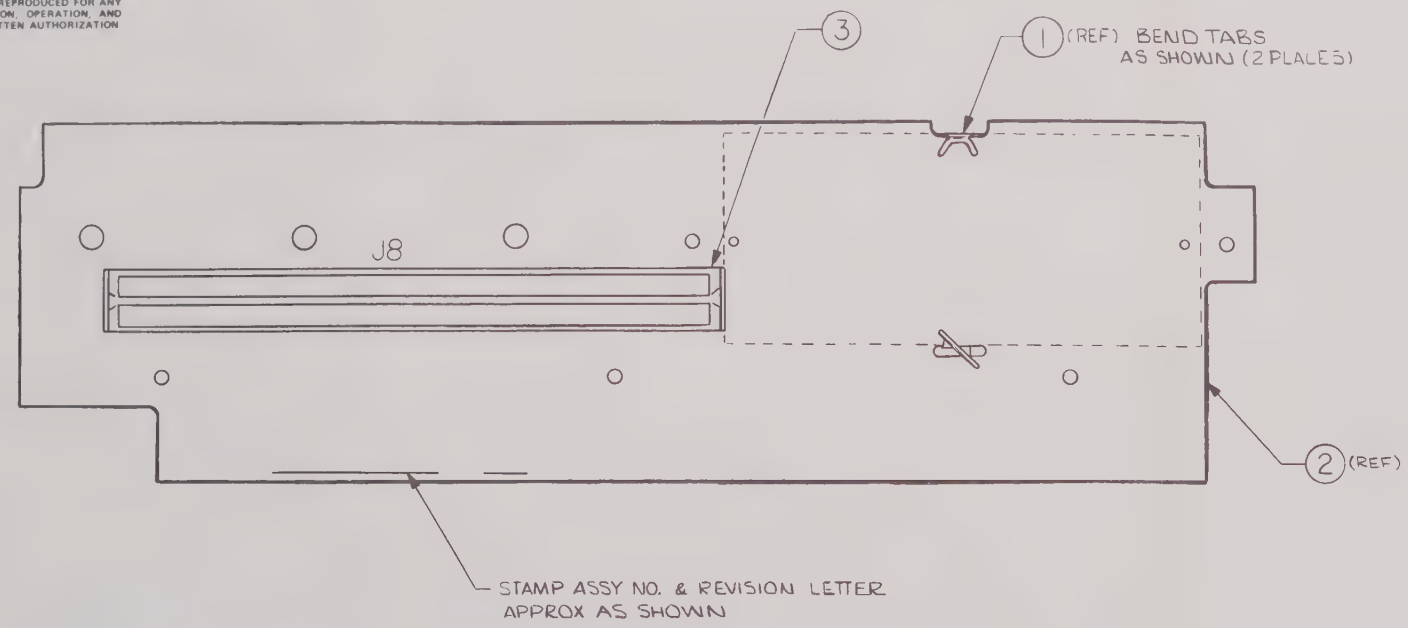
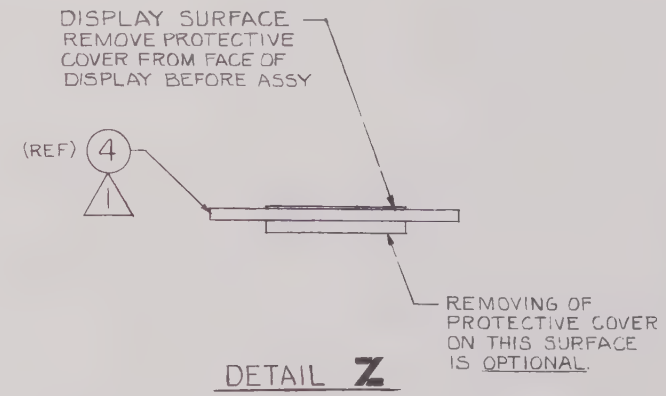
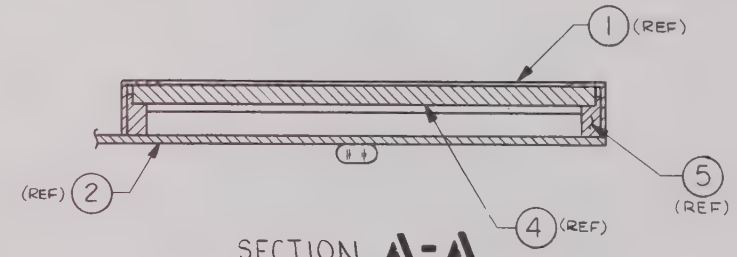
REV	ECN	BY	DATE	APP

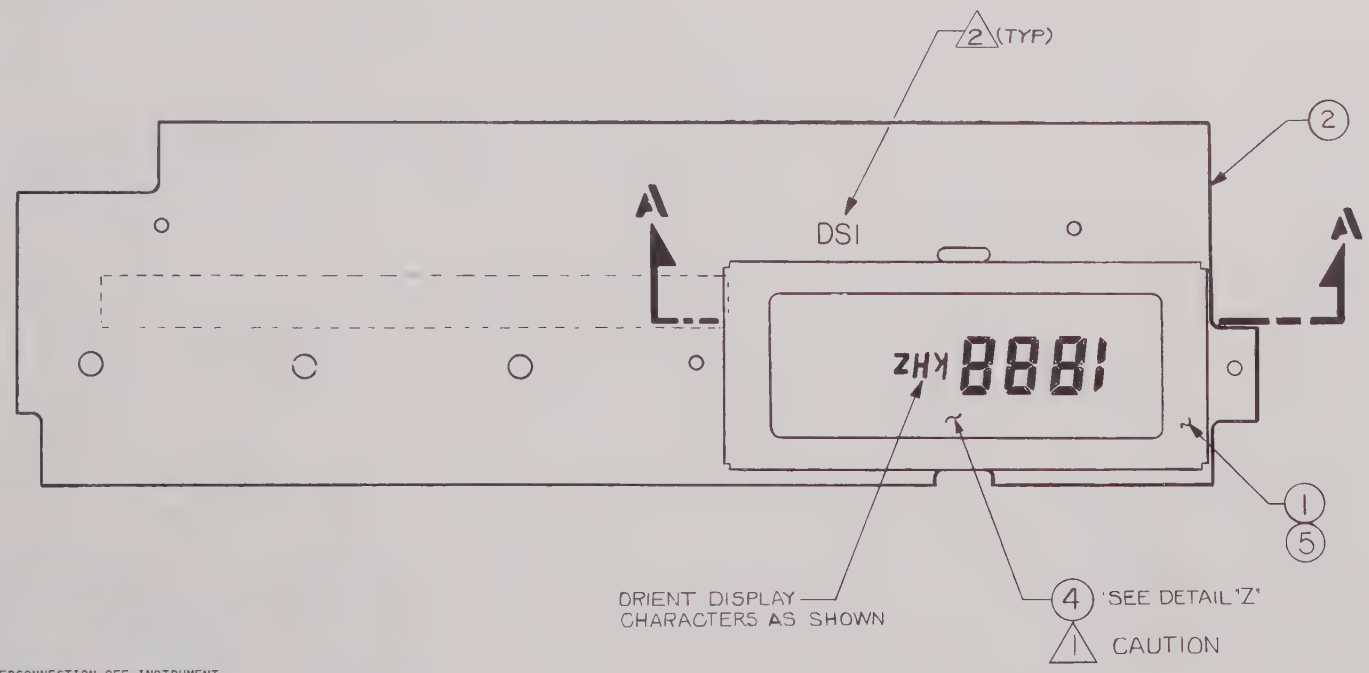



DISPLAY SURFACE REMOVE PROTECTIVE COVER FROM FACE OF DISPLAY BEFORE ASSY
(REF) 4
1
REMOVING OF PROTECTIVE COVER ON THIS SURFACE IS OPTIONAL.

DETAIL Z



SECTION A-A



4. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
3. SEE 0103-00-1117 FOR SCHEMATIC.
2. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A1A1. REFERENCE DESIGNATIONS DO NOT APPEAR ON ACTUAL PARTS.
1. CAUTION GLASS: LCD DISPLAY IS EXTREMELY FRAGILE. CARE MUST BE USED AS NOT TO CRACK GLASS DISPLAY.

NOTE UNLESS OTHERWISE SPECIFIED

REFERENCE DESIGNATORS	PART DESCRIPTION	DRIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, DISPLAY	0103-00-1117	WVTK	0103-00-1117	1
1	BEZEL, LCD	1400-01-6181	WVTK	1400-01-6183	1
2	DISPLAY BD	1700-00-1117	WVTK	1700-00-1117	1
3	CONNECTOR (70 PIN)	ETC35DRTN	SULIN	2100-02-0140	1
4	DISPLAY, LCD	2400-03-0012	WVTK	2400-03-0012	1
5	LCD CONNECTOR	09191-09	TECNT	2400-03-0013	1

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. MAGNOLIA	DATE 6-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PCA, DISPLAY (A1A1)
FINISH WAVETEK PROCESS	RELEASE APPROV 11/4/83		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 21/22	DWG NO 1208-00-1117 REV
	SCALE 2:1	CODE IDENT 23338	SHEET OF

12C8-GC-1117

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-3684

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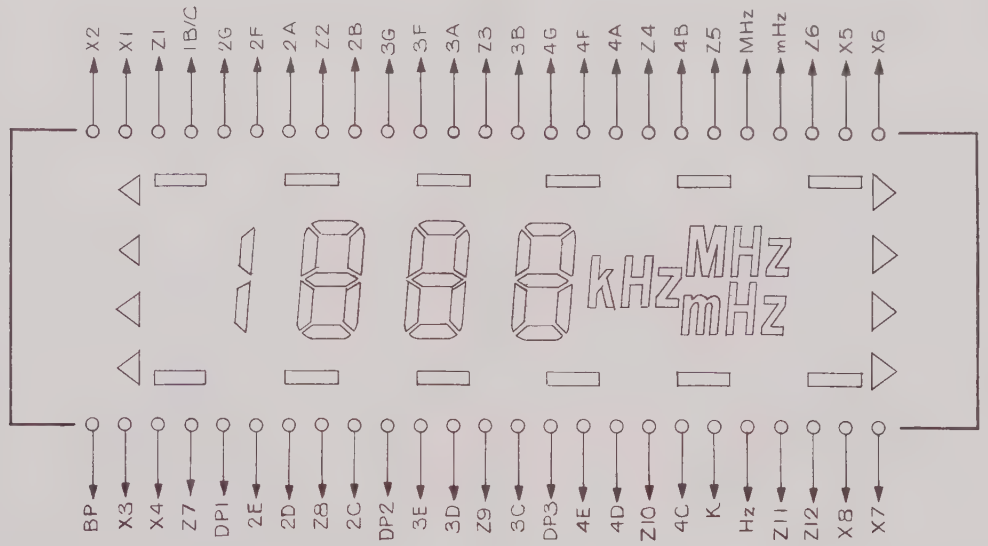
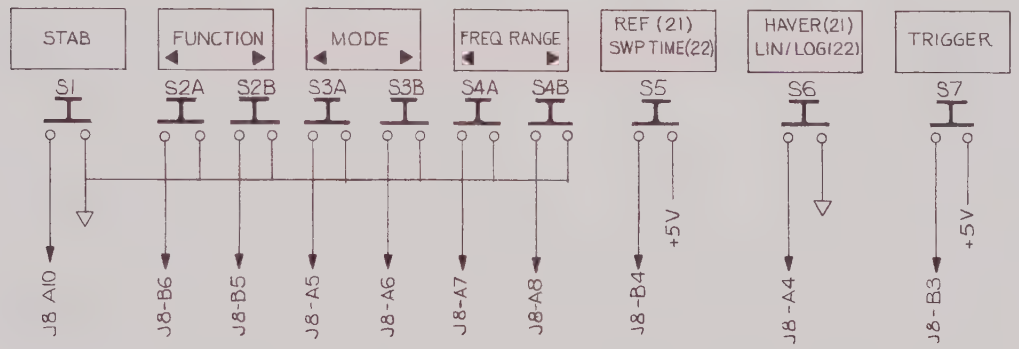
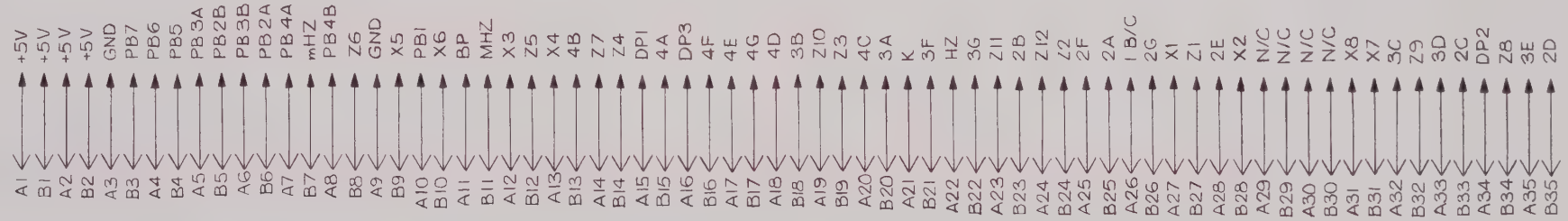
REV	ECN	BY	DATE	APP

DS1


X2 X1 Z1 1B/C 2G 2F 2A Z2 2B 3G 3F 3A Z3 3B 4G 4F 4A Z4 4B Z5 MHz mHz Z6 X5 X6
kHz MHz mHz
BP X3 X4 Z7 DP1 2E 2D Z8 2C DP2 3E 3D Z9 3C DP3 4E 4D Z10 4C K Hz Z11 Z12 X8 X7



J8



2. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A1A1.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A Talmadge	DATE 6/20/83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR —	12-19-83	TITLE: SCHEMATIC, DISPLAY (A1A1)
FINISH WAVETEK PROCESS —	RELEASE APPROV 11/4/83		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1 XX ± 030		
	DO NOT SCALE DWG	MODEL NO 21/22	DWG NO 0103-00-117 REV
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

0103-00-1117

BISHOP GRAPHICS/ACCUPRESS REORDER NO A3894

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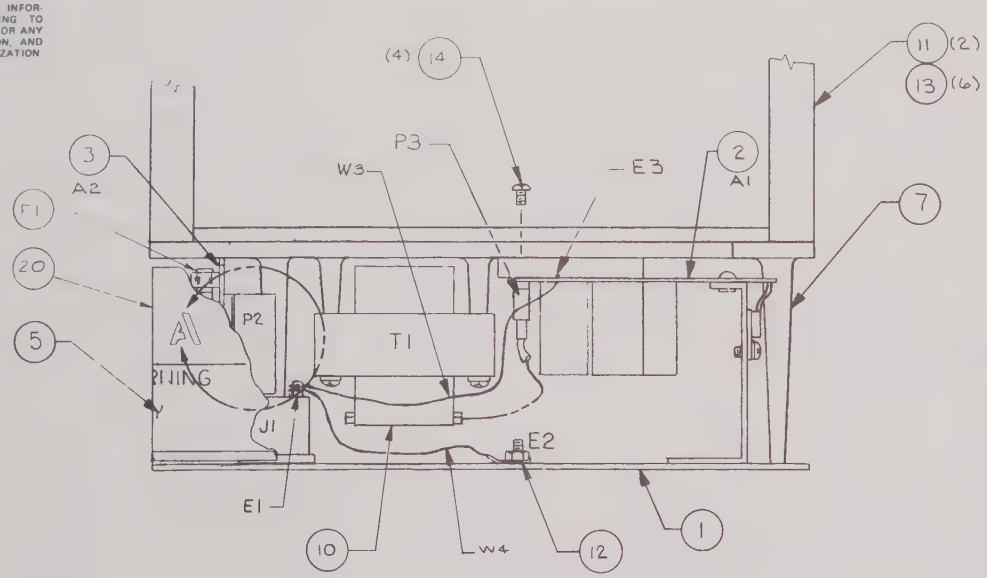
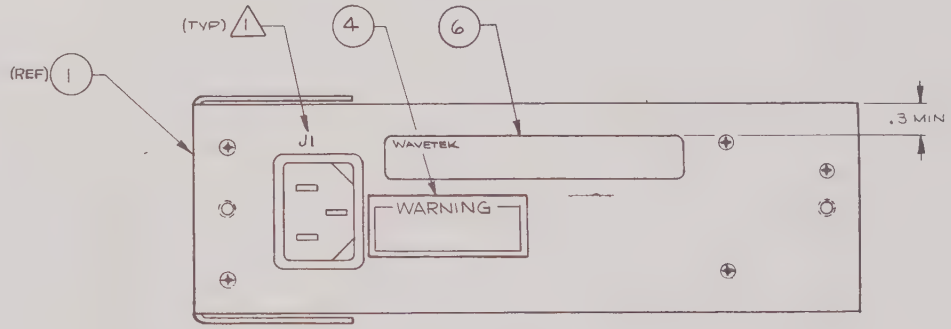
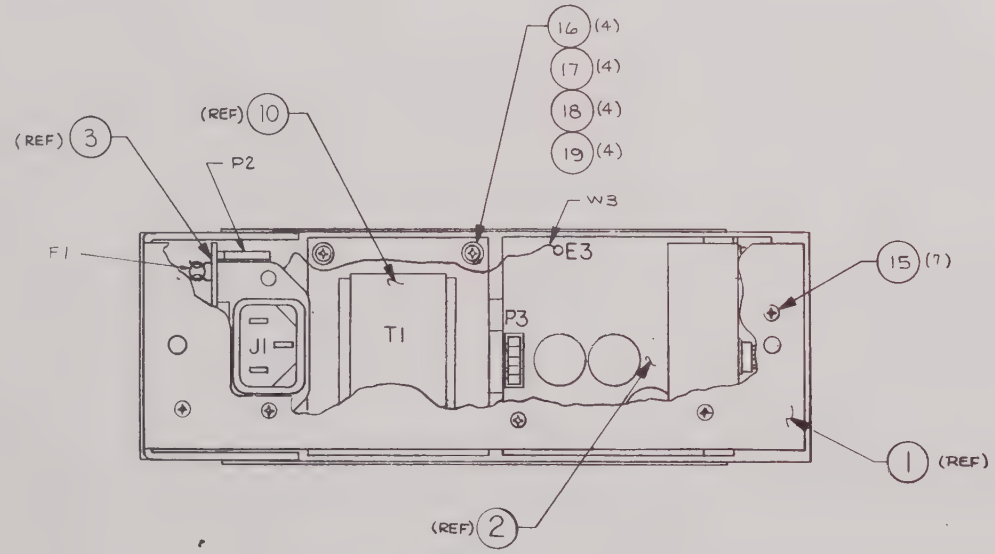
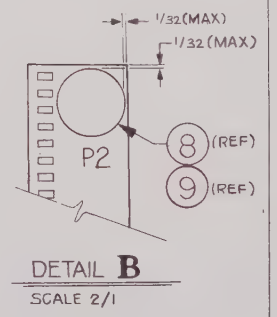
REV	ECN	BY	DATE	APP
A	ECN 4562	KA	1/25/85	
B	[illegible]			
C	[illegible]			
D	#6099	DAH	2/1/85	ART

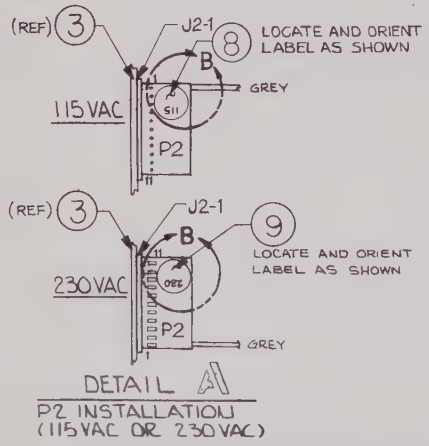








DETAIL **B**
SCALE 2/1



DETAIL **A**
P2 INSTALLATION
(115 VAC OR 230 VAC)

DETAIL 'A' { 115 VAC / 230 VAC

WIRING LIST		
FROM	TO	REF DES
E1	E2	W4
E1	E3	W3
P2 (1 THRU 11)	J2 (1 THRU 11)	—
P2 (11 THRU 1)	J2 (1 THRU 11)	—
P3 (1 THRU 5)	J3 (1 THRU 5)	—

4. WIRES & CABLES OBTAINED FROM CABLE KIT 1207-00-1120.
3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2. REFERENCE DESIGNATIONS DO NOT APPEAR ON ACTUAL PARTS.

NOTE UNLESS OTHERWISE SPECIFIED

LABEL INSTALLATION

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
20	ASSY, FUSE COVER	1201-00-1585	WVTK	1201-00-1585	1
1	ASSY, REAR PANEL	1201-00-1586	WVTK	1201-00-1586	1
10	TRANSFORMER	5600-00-0027	WVTK	1204-00-0061	1
2	PCA, POWER SUPPLY	21-1118	WVTK	1208-00-1118	1
3	PCA, AC PRIMARY	21-1119	WVTK	1208-00-1119	1
4	LABEL, WARNING	801-6940	WVTK	1400-00-6940	1
5	LABEL, CAUTION	859-1400	WVTK	1400-01-1400	1
6	LABEL, RATING	182A-4610	WVTK	1400-01-4610	1
7	PANEL, POWER SUPPLY MODIFIED	1400-01-6149	WVTK	1400-01-6149	1
8	LABEL, 115 VAC	21-6900	WVTK	1400-01-6900	1
9	LABEL, 230 VAC	21-6910	WVTK	1400-01-6910	1
11	PANEL, SIDE-23 (GPIB)	WVTK	23-8463	1400-01-8463	2
F1	FUSE, 3/8A, 250V, S-B	313.375	LITFU	2400-03-0009	1
12	NUT, FLEXLOCK, CAD I 6-32	6-32 NUT F.L.	CMRCL	2800-19-6100	1
13	SCREW, SELF TAPPING TYPE B, PAN CROSS	B-18 X 1/2	CMRCL	2800-22-8208	6
14	SCREW, SELF LOCKING, PAN CROSS RECESS	4-40 X 1/4	CMRCL	2800-23-4104	4
16	WASHER, FLAT, 6(.375 O.D.)	6 SAE FLAT WASHER	CMRCL	2800-26-6000	4
17	WASHER, FLAT, FIBER, #6	MS35338-136	COML	2800-28-6000	4
18	SCREW, PAN CROSS RECESS, 6-32X1 1/4	6-32 X 1 1/4	CMRCL	2800-38-6120	4
19	WASHER, SPLIT LOCK #6 6	#6SRLW	CMRCL	2800-42-6000	4
15	SCERW, F.H. 100 DEG CSK, CROSS RECESS4-40X3/8	4-40X3/8 F.H.	CMRCL	2800-44-4106	7

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. MAGNOLIA	DATE 6-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	10/19/83	TITLE ASSEMBLY, POWER SUPPLY (A2)
FINISH WAVETEK PROCESS	RELEASE APPROV	11-4-83	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ·010 ANGLES ·1 XX ·030		
	DO NOT SCALE DWG	MODEL NO 21/22	DWG NO 1101-00-1113 REV D
	SCALE 1/1 NOTED	CODE IDENT 23338	SHEET 1 OF 1

1101-00-1113 D

BISHOP GRAPHICS/ACCUPRESS REORDER NO A 3894

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REV	ECN	BY	DATE	APP
B	#4000, 4101	A.I.	[illegible]	- -
C	#4728	KA	7/10/85	A.S.T.
D	E6028	DAM	2/11/86	A.S.T.

A2 A2
PCA AC PRIMARY
1208-00-1119

F1		
MODEL	115	230
21/22	3/8 A	3/16 A
23	1/2 A	1/4 A
75	3/8 A	3/16 A

NOTE FOR 230V HOOK-UP INVERT CONNECTOR P2 AS SHOWN BELOW

J2-	P2-
1	11
2	10
3	9
4	8
5	7
6	6
7	5
8	4
9	3
10	2
11	1

A2 A1
PCA POWER SUPPLY
1208-00-1118 (MODEL 21/22/23)
1208-00-1772 (MODEL 75)

J32 1 2 3 4 5 6 7

J1 HOT NEUT GND

OFF ON S1

△4 F1

E1 E2 E3

GRN/YEL (W4)

(W3) GRN/YEL

(115V HOOK-UP)

J2-	P2-	
1		BLK
N.C.	2	
3		WHT/BLK
N.C.	4	
5		GRY
N.C.	6	
7		WHT/GRY
N.C.	8	
9		
10		
11		

A2 T1

P3-	J3-	
	2	RED
	3	WHT/RED
	1	RED
	5	BLU
	4	BLU

CR1 VM18

C1 .01 GAP

C2 1000/50V

C3 1000/50V

C4 4.7/50V

C5 4.7/50V

C6 .1/50V

C7 10/25V

C8 10/25V

C9 .01 GAP

C10 2200/16V

C11 .1

C12 .1

CR2 VSB54

RV1 V56ZA8

Q1 TIP29

Q2 TIP29

R1 △3

R2 △3

VR1 LM325A OR LM125

VR2 LM7805 (IN, OUT, COM)

+15V -15V +5V

J4-

A1	B1
A2	B2
A3	B3
A4	B4
A5	B5
A6	B6
A7	B7
A8	B8
A9	B9
A10	B10

J5-

A1	B1
A2	B2
A3	B3
A4	B4
A5	B5
A6	B6
A7	B7
A8	B8
A9	B9
A10	B10

J31 1 2 3 4 5 6

P32 1 2 3 4 5 6 7 P2 1 2 3 4 5 6 7 8 9 10 11

BLK		RED P3 2
ORN		WHT/RED 3
WHT/BLK		RED 1
GRY		BLU 5
VIO		BLU 4
WHT/GRY		

CONNECTIONS FOR TRANSFORMER WITH HI/LO AND 115/230V PRIMARIES

(SHOWN IN 115V, HI POSITION – REVERSE P32 FOR LO POSITION)

△4 FOR FUSE P/N SEE:
MODEL 21/22-1101-00-1113
MODEL 23-1101-00-1703
MODEL 75-1101-00-1771

△3. R1 AND R2 VALUES:
1Ω, 1/4W (MODEL 21/22/23)
1.5Ω, 1/2W (MODEL 75)

2. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC.

1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2.

NOTE UNLESS OTHERWISE SPECIFIED

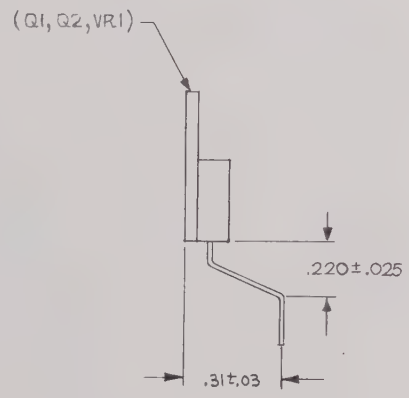
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 5-13-82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR [illegible]	11/4/82	TITLE: SCHEMATIC, POWER SUPPLY (A2)
FINISH WAVETEK PROCESS —	RELEASE APPROV [illegible]	11/4/83	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 21/22
	SCALE —		DWG NO 0103-00-1113 REV D
			CODE IDENT 23338 SHEET 1 OF 1

0103-00-1113

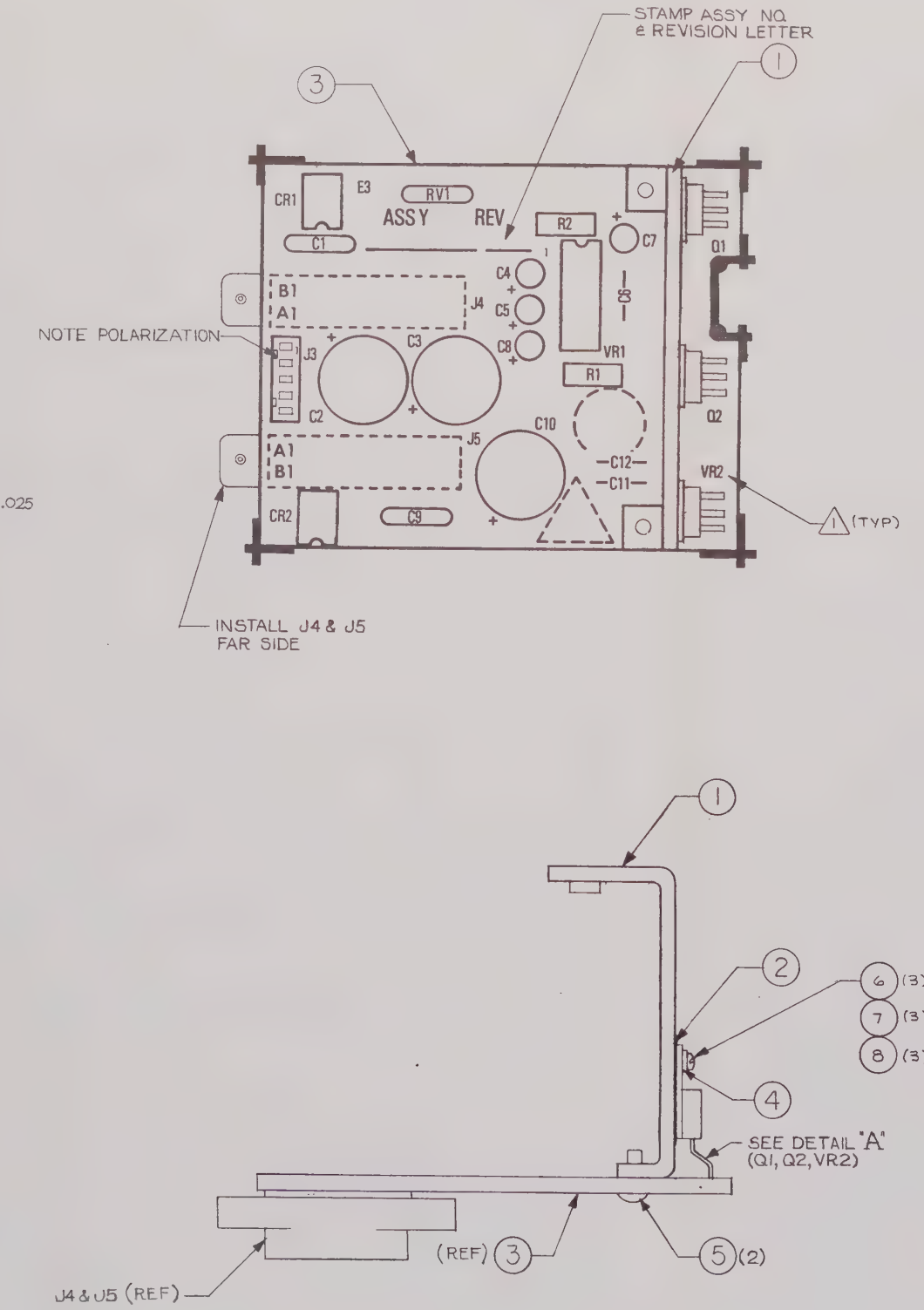
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP
B				



DETAIL A
(SCALE: NONE)



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
NONE	ASSY, HEATSINK BRACKET	75-2251	WVTK	1206-00-2251	1
C1 C9	CAP, CER, .01MF, 1KV	GAP-103	CRL	1500-01-0309	2
C11 C12 C6	CAP, CER, MN, .1MF, 50V, Z 5U, +80/-20% RAD LD SP .2	5028ES50RD104Z	KYCRA	1500-01-0420	3
C7 C8	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	CRE SERIES 10/25	CAPAR	1500-31-0002	2
C2 C3	CAP, ELECT, 1000MF/50V RADIAL LEAD, SP .30	CRE SERIES 1000/50	CAPAR	1500-31-0203	2
C10	CAP, ELECT, 2200MF, 16V RADIAL LEAD, SP .30	CRE SERIES 2200/16	CAPAR	1500-32-2201	1
C4 C5	CAP, ELECT, 4.7MF/50V RADIAL LEAD, SP .10	CLE SERIES 4.7/50	CAPAR	1500-34-7903	2
2	POWER SUPPLY BD	21-1118	WVTK	1700-00-1118	1
J4 J5	CONNECTOR(20 PIN)	ETCIODRTI	BULIN	2100-02-0139	2
J3	HEADER, CONN(5 PIN)	102202-2	AMP	2100-02-0143	1
J31	CONN, HEADER, 6 PIN	640098-6	AMP	2100-02-0170	1
3	WASHER	B51547F015	MOT	2800-11-0015	3

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, POWER SUPPLY	1208-00-1772	
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
4	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	2
5	SCREW, SELF TAPPING TYPE B, PAN CROSS	4-24 X 3/8	CMRCL	2800-22-4162	3
6	WASHER, FLAT, 4(.209 O.D.)	NAS620-4	CMRCL	2800-26-4001	3
7	WASHER, SPLIT LOCK, 4	#4SRLW	CMRCL	2800-42-4000	3
8	INSULATOR(TO-220)	60-11-8302-1674	CHOMR	3100-00-0010	3
R1 R2	RES, CAR, 1/2W, 5%, 1.5	RC-1/2-1R5J	STKPL	4700-25-0159	2
RV1	VARISTOR	4899-00-0045	WVTK	4799-00-0048	1
CR1 CR2	DIODE, BRIDGE	VM18	VARO	4801-02-0008	2
Q1 Q2	TRANS	TIP-29	TI	4902-00-0290	2
VR1	IC, VOLTAGE REGULATOR	LM325A	NSC	7000-03-2301	1
VR2	VOLTAGE REGULATOR	MA7805UC	FAIR	8000-78-0500	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, POWER SUPPLY	1208-00-1772	
		PAGE 2	

3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2A1.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 6/1/83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR		TITLE PCA, POWER SUPPLY (A2A1)
FINISH WAVETEK PROCESS —	RELEASE APPROV L. McL. 11/3 83		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1		
	DO NOT SCALE DWG		MODEL NO 21/22
	SCALE 2/1		DWG NO 1208-00-1118 REV B
			CODE IDENT 23338 SHEET 1 OF 1

1208-00-1118 B

BISHOP GRAPHICS/ACCUPRESS REORDER NO A 3894

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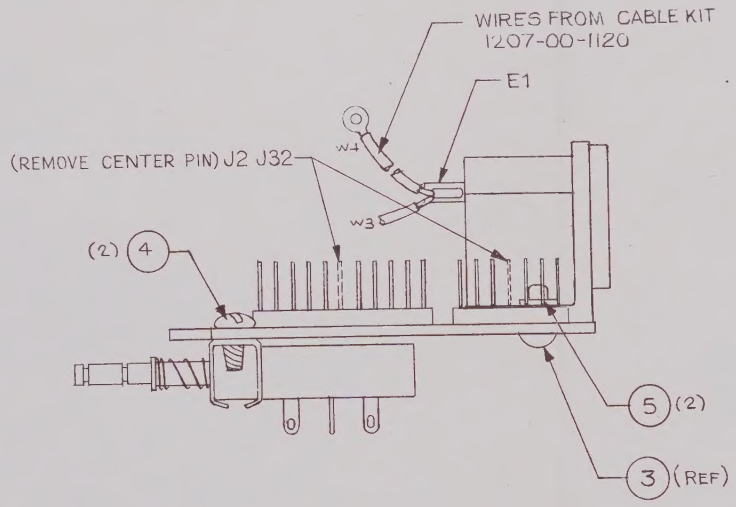
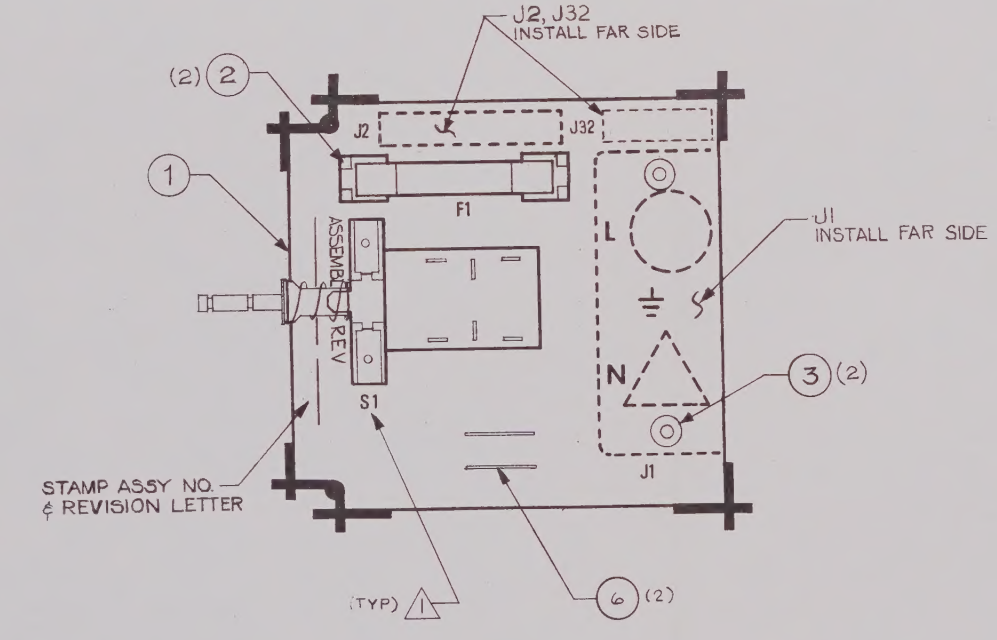
REV	ECN	BY	DATE	APP
A	#2F1454&4250		1/14/65	
	#4595		8/25/65	





REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
1	AC PRIMARY BD	21-1119	WVTK	1700-00-1119	1
J2	HEADER, CONN(11 PIN)	1-87224-1	AMP	2100-02-0144	1
J32	CONN, HEADER, UNSHROUDED, 7 PIN	87224-7	AMP	2100-02-0184	1
J1	RECEPT, POWER(PC)	EAC-303	SWCFT	2100-03-0069	1
2	FUSE HOLDER, CLIP	102071	LITFU	2400-05-0031	2
3	RIVET, ALUM 5/16X1/8 DIA .188-250	1125-0410	CHOBT	2800-12-0047	2
4	SCREW, S/T TYPE B, PAN CROSS RECESS, 4-24X1/4	4-24 X 1/4	CMRCL	2800-22-4142	2
5	WASHER, FLAT, #4(.312 O.D.)	#4FW	CMRCL	2800-26-4000	2
6	RESISTOR, 0 OHM JUMPER	JP02T680	ROHM	4799-00-0087	2
S1	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1

WAVETEK PARTS LIST	TITLE: PCA, AC PRIMARY	ASSEMBLY NO. 1208-00-1119	REV B

PAGE 1

3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2A2.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 6/13/83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PCA, AC PRIMARY (A2A2)
	RELEASE APPROV	6/13/83	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 21/22 / DWG NO 1208-00-1119 / REV B
	SCALE 2/1		CODE IDENT 23338 / SHEET 1 OF 1

1208-00-8021 B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-8894

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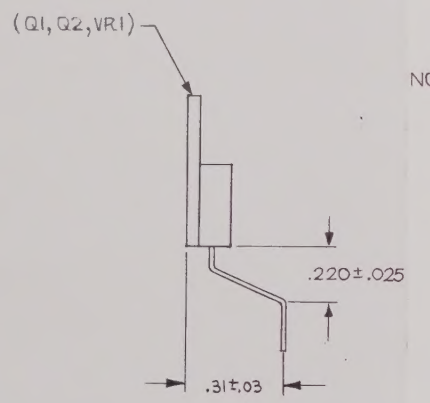
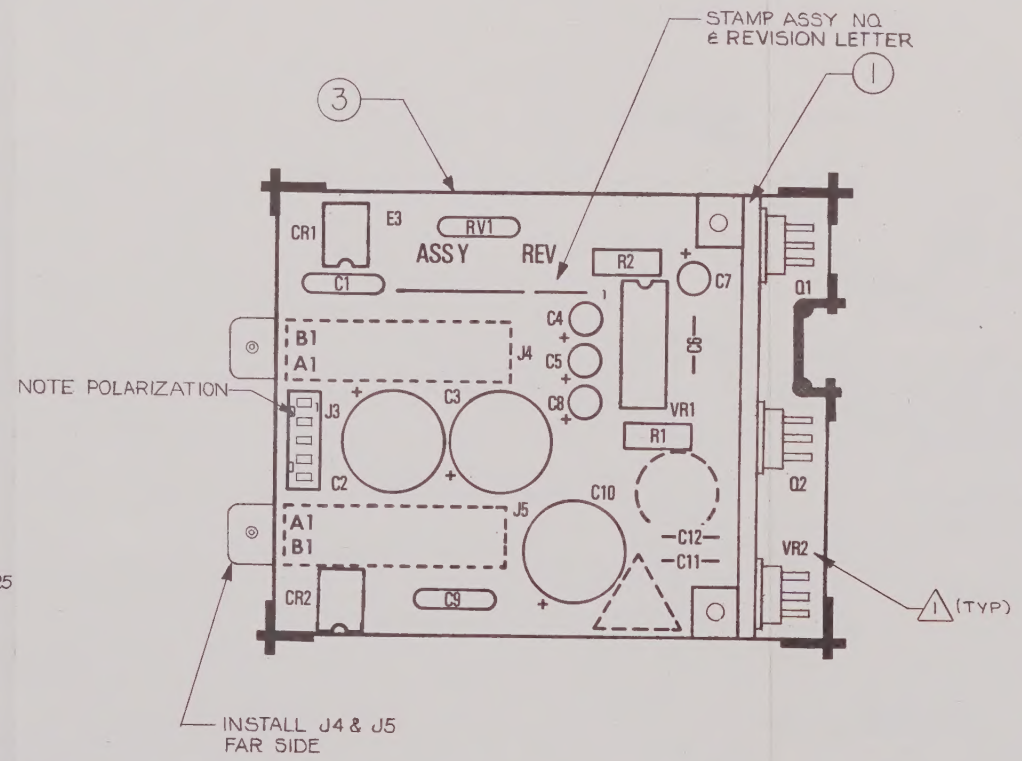
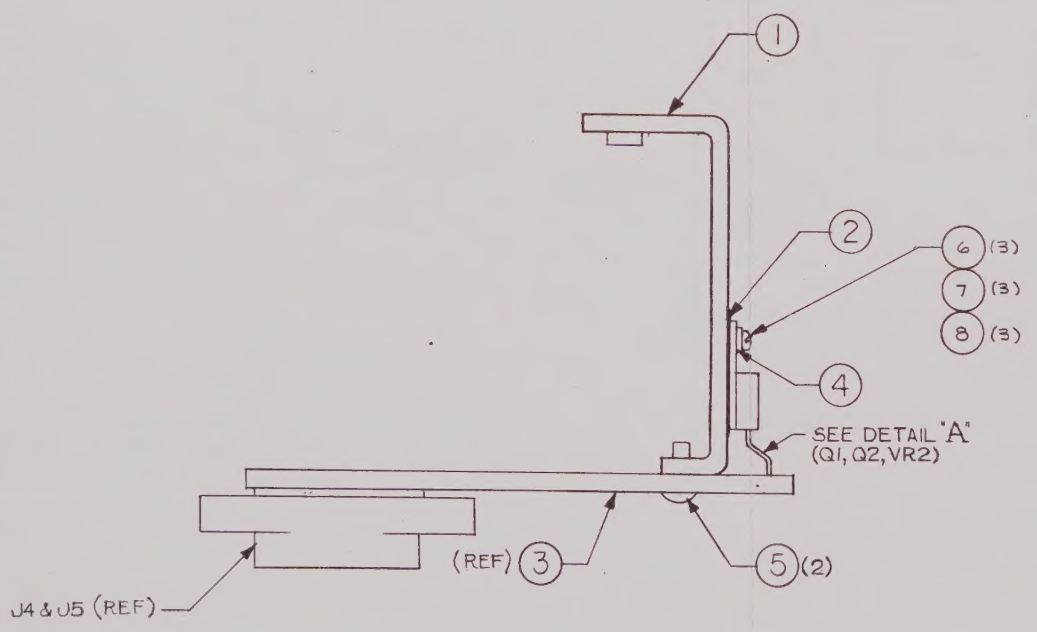
REV	ECN	BY	DATE	APP
A	[illegible]	MF	11/21/85	
B	#4728	KA	7/19/85	



DETAIL A
(SCALE: NONE)





REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
NONE	ASSY, HEATSINK BRACKET	75-2251	WVTK	1206-00-2251	1
C1 C9	CAP, CER, .01MF, 1KV	GAP-103	CRL	1500-01-0309	2
C11 C12 C6	CAP, CER, MN, .1MF, 50V, Z 5U, +80/-20% RAD LD SP .2	5028ES50RD104Z	KYCRA	1500-01-0420	3
C7 C8	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	CRE SERIES 10/25	CAPAR	1500-31-0002	2
C2 C3	CAP, ELECT, 1000MF/50V RADIAL LEAD, SP .30	CRE SERIES 1000/50	CAPAR	1500-31-0203	2
C10	CAP, ELECT, 2200MF, 16V RADIAL LEAD, SP .30	CRE SERIES 2200/16	CAPAR	1500-32-2201	1
C4 C5	CAP, ELECT, 4.7MF/50V RADIAL LEAD, SP .10	CLE SERIES 4.7/50	CAPAR	1500-34-7903	2
2	POWER SUPPLY BD	21-1118	WVTK	1700-00-1118	1
J4 J5	CONNECTOR(20 PIN)	ETCIODRTI	SULIN	2100-02-0139	2
J3	HEADER, CONN(5 PIN)	102202-2	AMP	2100-02-0143	1
J31	CONN, HEADER, 6 PIN	640098-6	AMP	2100-02-0170	1
3	WASHER	B51547F015	MOT	2800-11-0015	3

WAVETEK PARTS LIST | TITLE: PCA, POWER SUPPLY | ASSEMBLY NO.: 1208-00-1772 | REV:

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
4	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	2
5	SCREW, SELF TAPPING TYPE B, PAN CROSS	4-24 X 3/8	CMRCL	2800-22-4162	3
6	WASHER, FLAT, 4(.209 O.D.)	NAS620-4	CMRCL	2800-26-4001	3
7	WASHER, SPLIT LOCK, 4	#4SRLW	CMRCL	2800-42-4000	3
8	INSULATOR(TO-220)	60-11-8302-1674	CHOMR	3100-00-0010	3
R1 R2	RES, CAR, 1/2W, 5%, 1.5	RC-1/2-1R5J	STKPL	4700-25-0159	2
RV1	VARISTOR	4899-00-0045	WVTK	4799-00-0048	1
CR1 CR2	DIODE, BRIDGE	VM18	VARO	4801-02-0008	2
Q1 Q2	TRANS	TIP-29	TI	4902-00-0290	2
VR1	IC, VOLTAGE REGULATOR	LM325A	NSC	7000-03-2501	1
VR2	VOLTAGE REGULATOR	MA7805UC	FAIR	8000-78-0500	1

WAVETEK PARTS LIST | TITLE: PCA, POWER SUPPLY | ASSEMBLY NO.: 1208-00-1772 | REV:

3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2A1.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: A.TALMADGE	DATE: 6/1985	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL: #	PROJ ENGR: [illegible]		TITLE: PCA, POWER SUPPLY (A 2A1)
FINISH: WAVETEK PROCESS #	RELEASE APPROV: [illegible] 11/4/85		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX: .010 ANGLES: ±1 XX: .030		
	DO NOT SCALE DWG	SCALE: 2/1	MODEL NO: 21/22 · DWG NO: 1208-00-1118 · REV: B
			CODE IDENT: 23338 · SHEET 1 OF 1

1208-00-1118 B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

MP MASTER
MA35620